

Compal Confidential

ULC AMD M/B LA-A996P DIS Schematics Document

AMD APU Beema/Kabini FT3 + ATI SUN LE + DDR3

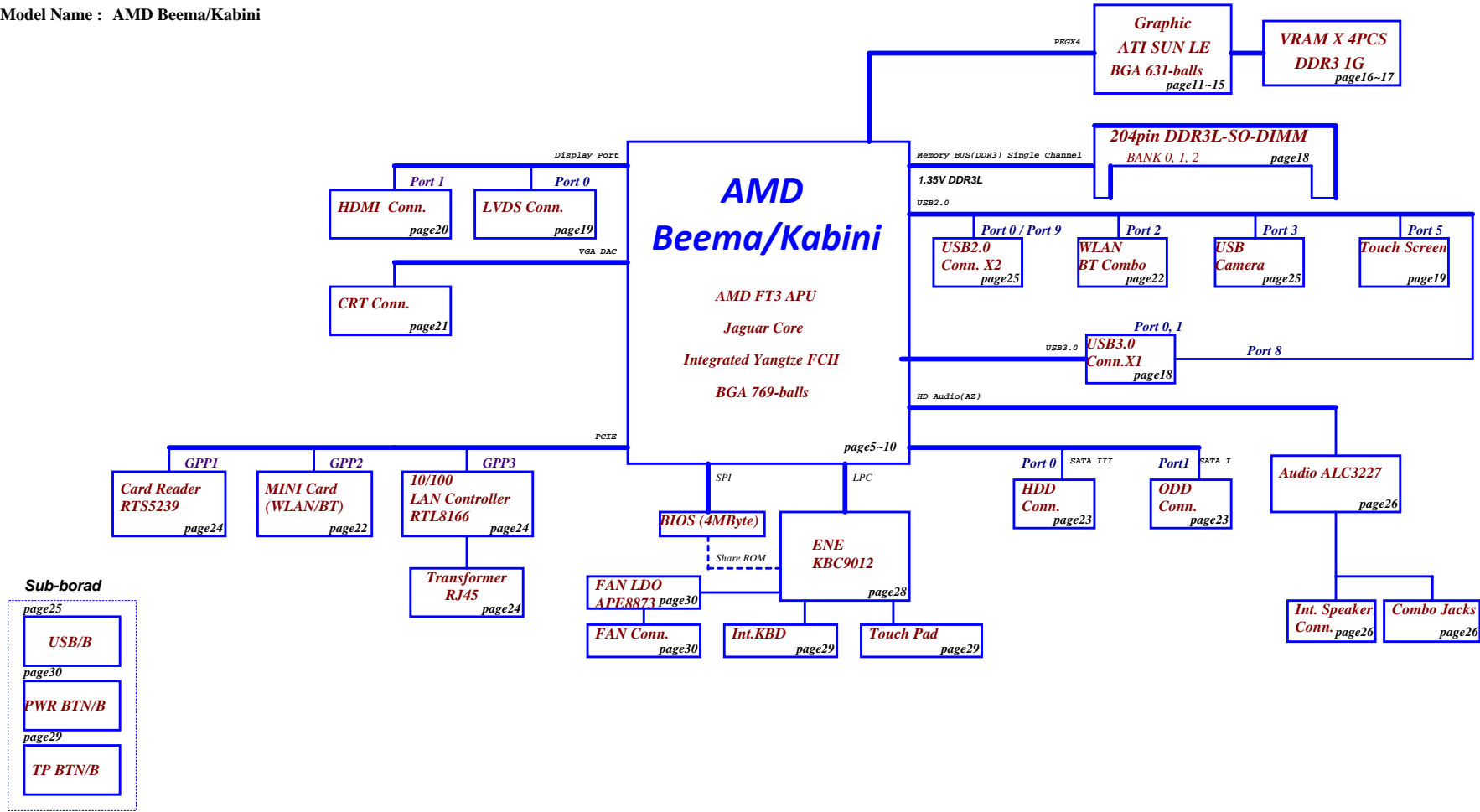
Project Code : ZSO51

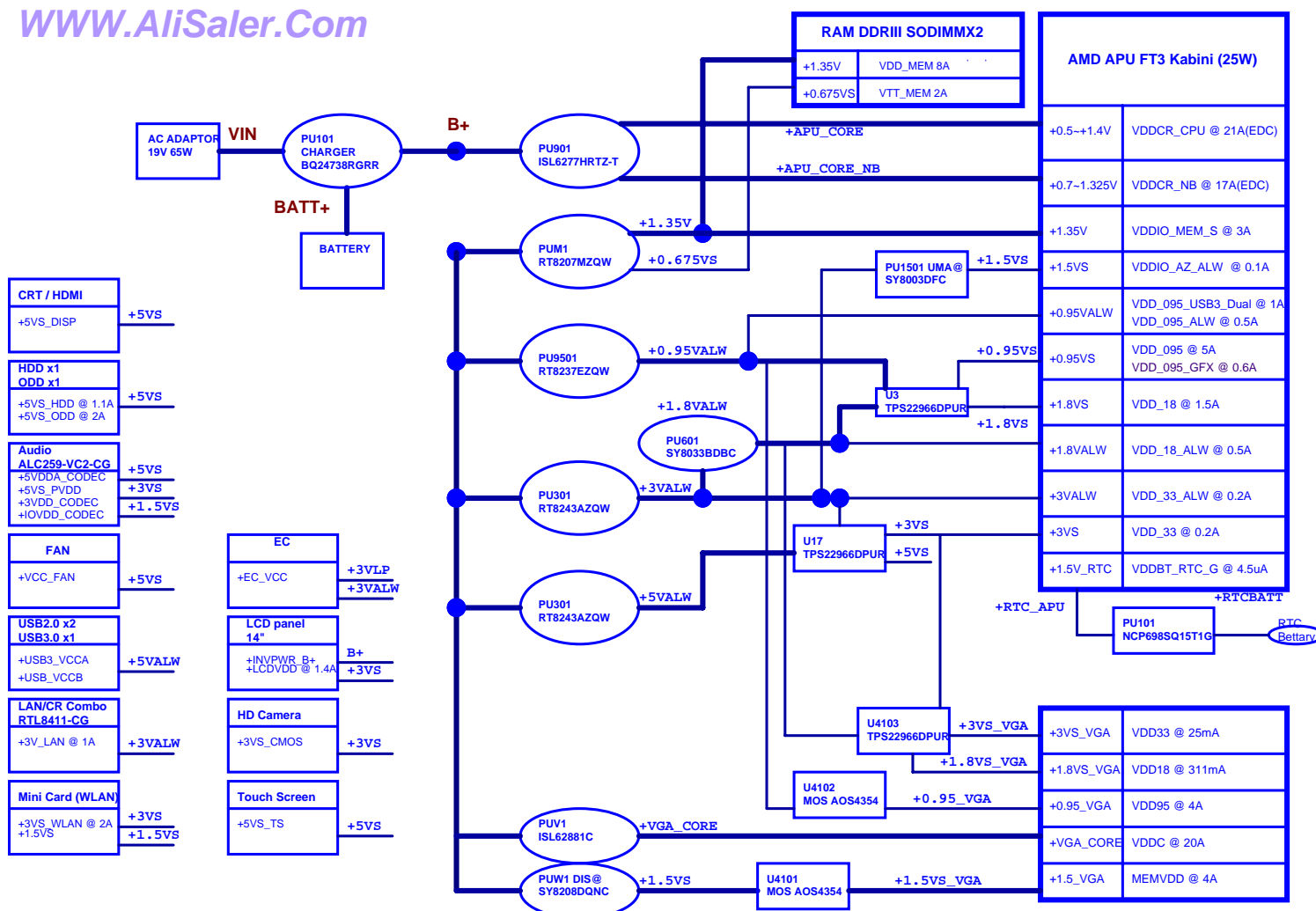
2014/02/08

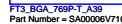
PV Rev. 4.0

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				C	0.1
				Document Number	
				LA-A996P	
				Date:	Monday, February 17, 2014
				Sheet	1 of 46

Model Name : AMD Beema/Kabini







Rev	0.1
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[illegible]

4MB SPI ROM & Non-share ROM.

0.1u, 0402_25V6 2 CC14 1 +3VALW

Check CS# PU R 1k0r10k and pop/nopop SCL v1.20 : If an SPI ROM is shared between the FCH and the Embedded Controller a 15-K pull-up resistor to +3.3V_SS is installed.

W25Q64FVSSIG, S08 SA000038P10

STIC FL 64M W25Q64FVSSIQ SOIC 8P SPI ROM SA000038A30

Support Share ROM

15, 09D4, 8P4R, 5% 4 5 3 6 2 7 1 8

FCH_SPI_MOSI# 4 EC_SPI_SI 28 EC_SPI_CS0# 28

FCH_SPI_CS# 1 2 EC_SPI_SO 28

FCH_SPI_HOLD# 3 4 EC_SPI_CLK 28

FCH_SPI_CLK 1 EC_SPI_CLK 28

Close to ROM

RC78, RC82 CNG to 0ohm 0903 SI

STRAPS OF APU

	LPC_FRAME#	LPC_CLK0_EC	LPC_CLK1	GEVENT2_L	RTC_CLK
H	SPI ROM (DEFAULT)	BOOT FAIL TIMER ENABLED	CLKGEN ENABLE (DEFAULT)	1.8V SPI ROM	NORMAL POWR UP/RESET TIMING (DEFAULT)
L	LPC ROM	BOOT FAIL TIMER DISABLED (DEFAULT)	CLKGEN DISABLED	3.3V SPI ROM (DEFAULT)	FAST POWER UP/RESET TIMING FOR SIMULATION

+3VALW

2 RC78 1 10K 0402_5% LPC_FRAME#

2 RC78 1 10K 0402_5% LPC_CLK0_EC

2 RC78 1 10K 0402_5% LPC_CLK1

1 RC78 1 2K 0402_5% LPC_FRAME#

1 RC78 1 2K 0402_5% LPC_CLK0_EC

1 RC78 1 2K 0402_5% LPC_CLK1

Security Classification: Compal Secret Data

Issued Date: 2013/02/26

Deciphered Date: 2015/07/06

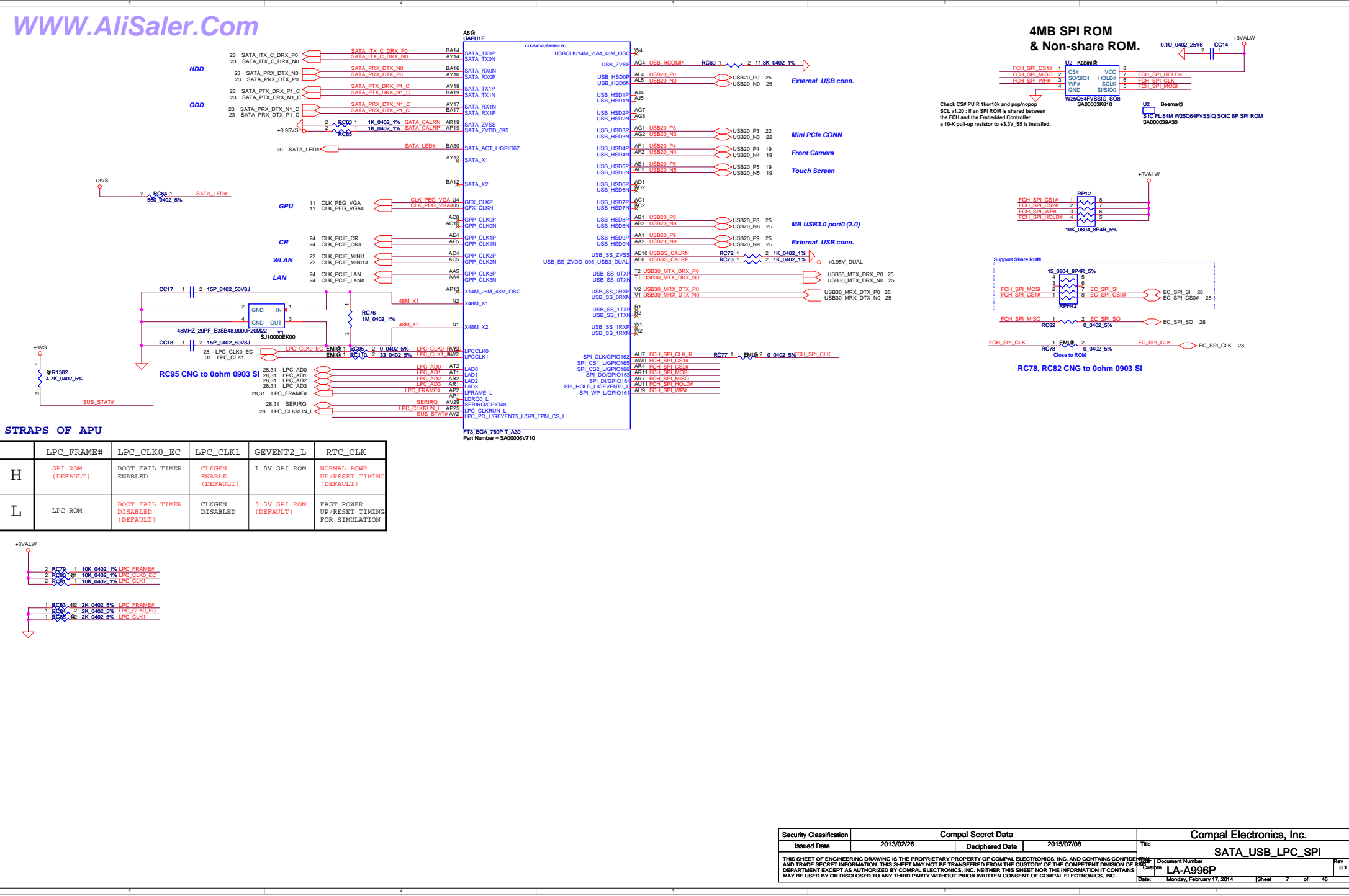
Title: SATA_USB_LPC_SPI

Document Number: LA-A996P

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Rev: 0.1

[illegible]

WWW.AliSaler.Com

4MB SPI ROM & Non-share ROM.

0.1u, 0402_25V6 2 CC14 1 +3VALW

Check CS# PU R 1k0r10k and pop/nopop SCL v1.20 : If an SPI ROM is shared between the FCH and the Embedded Controller a 15-K pull-up resistor to +3.3V_SS is installed.

W25Q64FVSSIG, S08 SA000038P10

STIC FL 64M W25Q64FVSSIQ SOIC 8P SPI ROM SA000038A30

Support Share ROM

15, 0804_8P4R_5% 4 5 3 6 2 7 1 8

FCH_SPI_CS# 1 2 3 4 5 6 7 8

FCH_SPI_MISO 1 2 3 4 5 6 7 8

FCH_SPI_MOSI 1 2 3 4 5 6 7 8

FCH_SPI_HOLD# 1 2 3 4 5 6 7 8

EC_SPI_SI 28

EC_SPI_CS0# 28

EC_SPI_SO 28

EC_SPI_CLK 28

Close to ROM

RC78, RC82 CNG to 0ohm 0903 SI

STRAPS OF APU

	LPC_FRAME#	LPC_CLK0_EC	LPC_CLK1	GEVENT2_L	RTC_CLK
H	SPI ROM (DEFAULT)	BOOT FAIL TIMER ENABLED	CLKGEN ENABLE (DEFAULT)	1.8V SPI ROM	NORMAL POWR UP/RESET TIMING (DEFAULT)
L	LPC ROM	BOOT FAIL TIMER DISABLED (DEFAULT)	CLKGEN DISABLED	3.3V SPI ROM (DEFAULT)	FAST POWER UP/RESET TIMING FOR SIMULATION

Security Classification: Compal Secret Data

Issued Date: 2013/02/26

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Title: SATA_USB_LPC_SPI

Document Number: LA-A996P

Customer: Monday, February 17, 2014

Sheet: 7 of 46

[illegible]

WWW.AliSaler.Com

4MB SPI ROM & Non-share ROM.

0.1u_0402_25V6 2 CC14 1 +3VALW

Check CS# PU R 1k0r10k and pop/nopop SCL v1.20 : If an SPI ROM is shared between the FCH and the Embedded Controller a 15-K pull-up resistor to +3.3V_SS is installed.

Support Share ROM

15 0904_8P4R_5% 4 5 3 6 2 7 8 EC_SPL_SI 28 EC_SPL_CS0# 28 FCH_SPL_MISO 1 FCH_SPL_CS1# 1 FCH_SPL_CS2# 2 FCH_SPL_CS3# 3 FCH_SPL_HOLD# 4 FCH_SPL_HOLD# 5

RP12 8 7 6 5 10K_0804_8P4R_5% RP102 1 2 EC_SPL_SO 0.0402_5% EC_SPL_CLK 28 EC_SPL_CLK 28

RC78, RC82 CNG to 0ohm 0903 SI

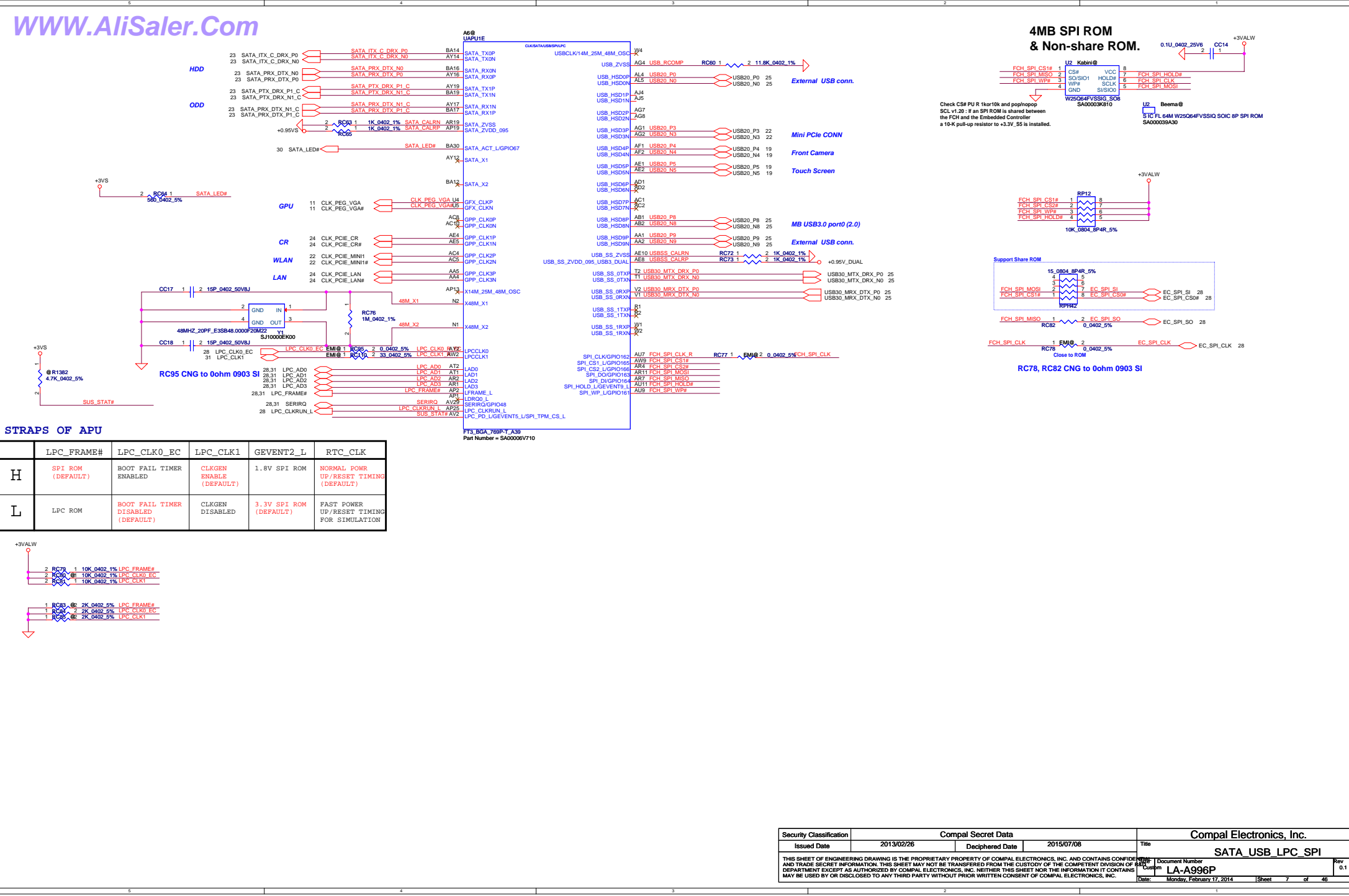
STRAPS OF APU

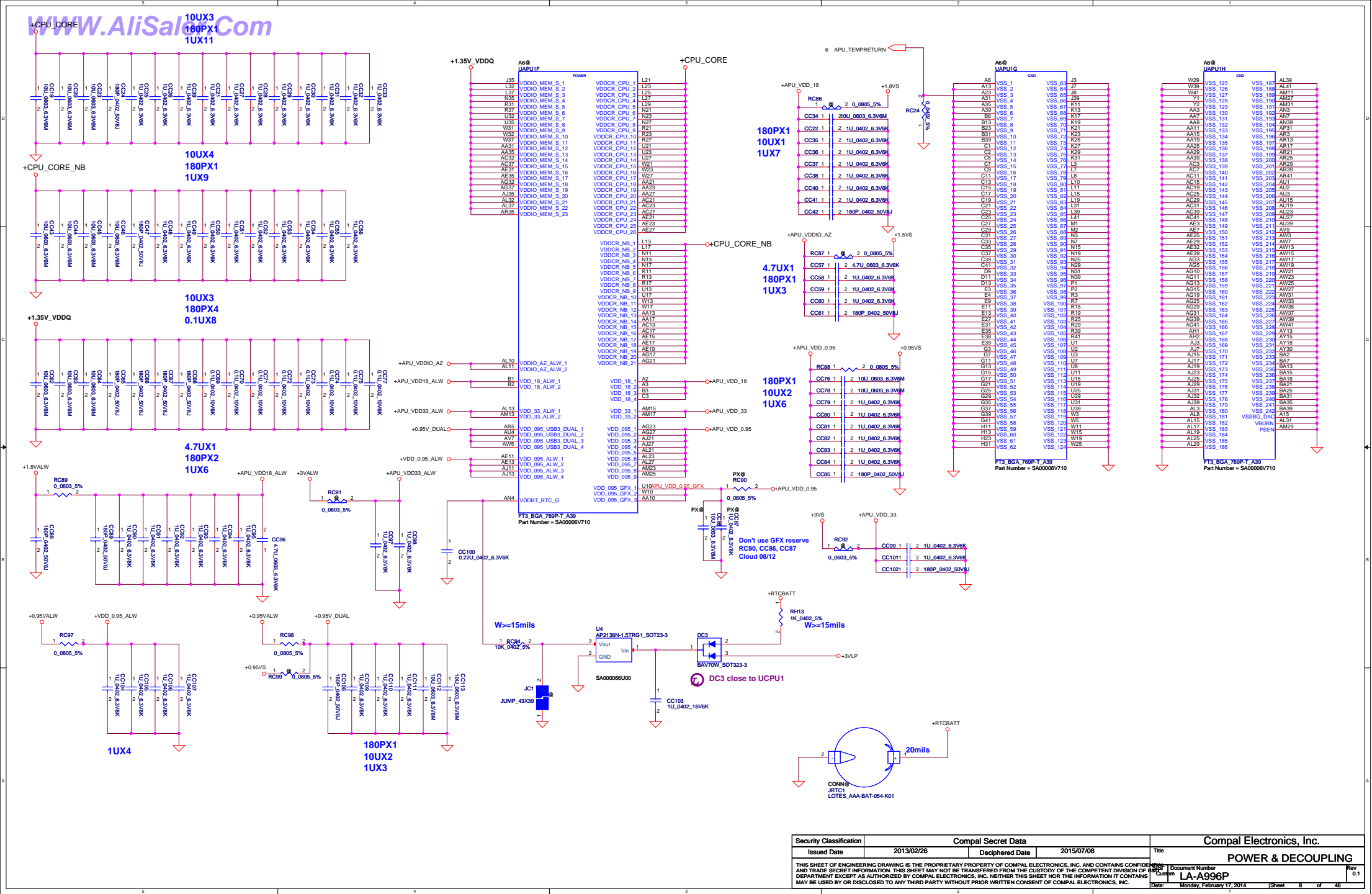
	LPC_FRAME#	LPC_CLK0_EC	LPC_CLK1	GEVENT2_L	RTC_CLK
H	SPI ROM (DEFAULT)	BOOT FAIL TIMER ENABLED	CLKGEN ENABLE (DEFAULT)	1.8V SPI ROM	NORMAL POWR UP/RESET TIMING (DEFAULT)
L	LPC ROM	BOOT FAIL TIMER DISABLED (DEFAULT)	CLKGEN DISABLED	3.3V SPI ROM (DEFAULT)	FAST POWER UP/RESET TIMING FOR SIMULATION

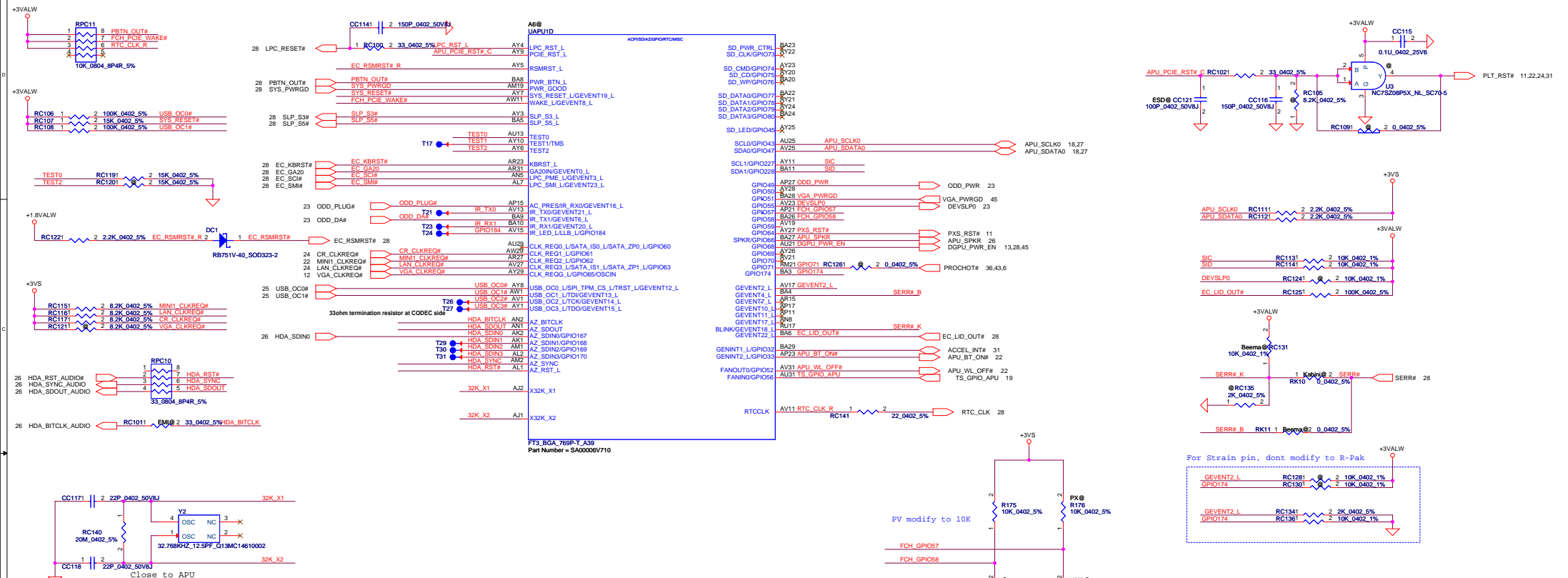
+3VALW 2 RC78 1 10K_0402_1% LPC_FRAME# 2 RC82 1 10K_0402_1% LPC_CLK0_EC 2 RC82 1 10K_0402_1% LPC_CLK1

1 RC78 1 2K_0402_5% LPC_FRAME# 1 RC82 1 2K_0402_5% LPC_CLK0_EC 1 RC82 1 2K_0402_5% LPC_CLK1

FTS_BGA_768P_Y_A39 Part Number = SA00006V710

[illegible]





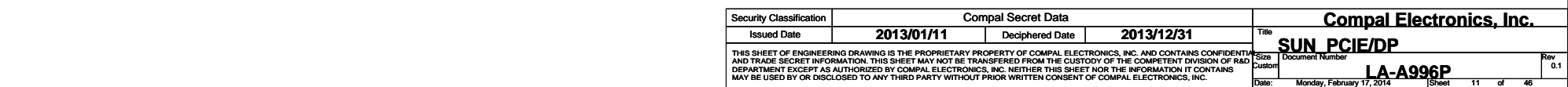
	<i>GPIO58</i>	<i>GPIO57</i>
<i>ZSO41</i> <i>14" UMA</i>	<i>L</i> <i>(R188)</i>	<i>L</i> <i>(R189)</i>
<i>ZSO41</i> <i>14" DIS</i>	<i>L</i> <i>(R188)</i>	<i>H</i> <i>(Internal PH)</i>
<i>ZSO51</i> <i>15" UMA</i>	<i>H</i> <i>(Internal PH)</i>	<i>L</i> <i>(R189)</i>
<i>ZSO51</i> <i>15" DIS</i>	<i>H</i> <i>(Internal PH)</i>	<i>H</i> <i>(Internal PH)</i>

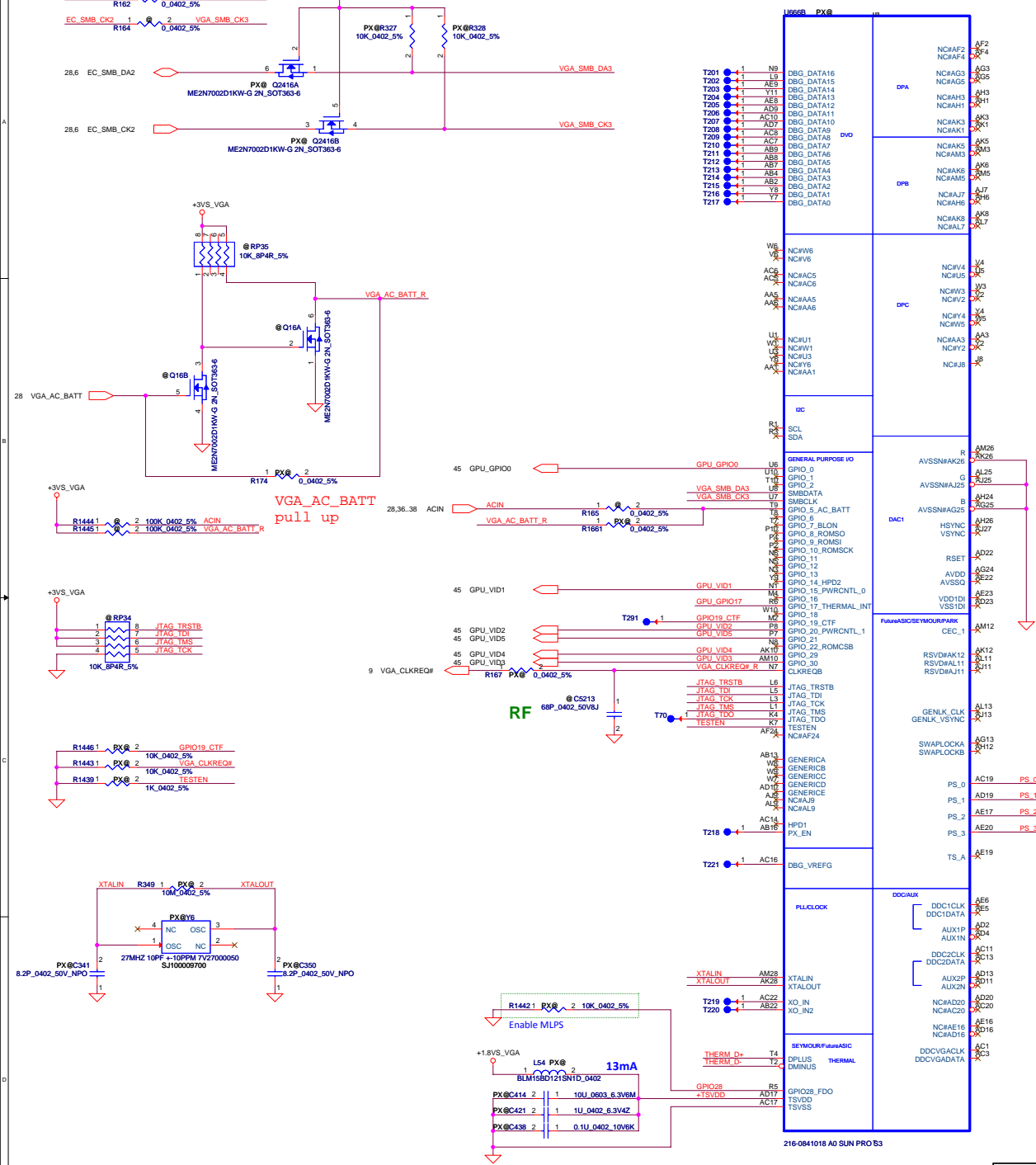
Panel ENBKL

Panel ENVDD

Panel PWM

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Issued Date	2013/02/26	Deciphered Date	2015/07/08	Level Shifter	
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				Date: Monday, February 17, 2014	Sheet 10 of 46

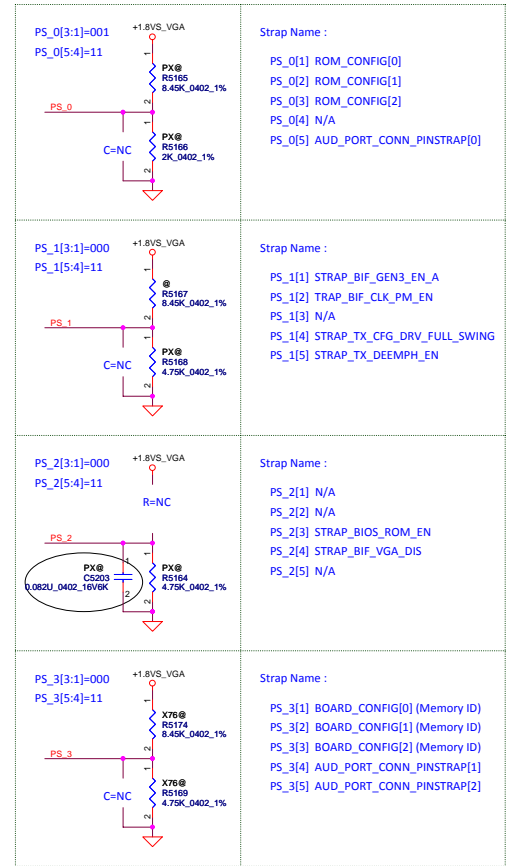




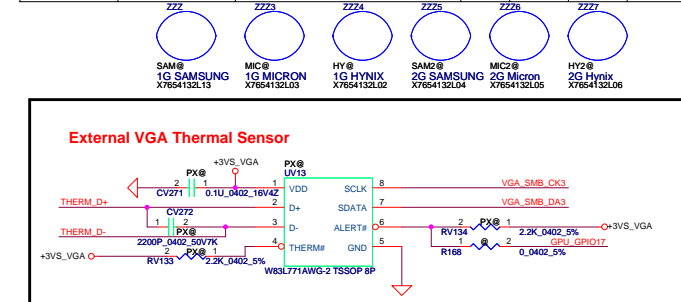
R _{pu} (ohm)	R _{pd} (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

0402 1% resistors are required

Capacitor Divider Lookup Table	
Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11



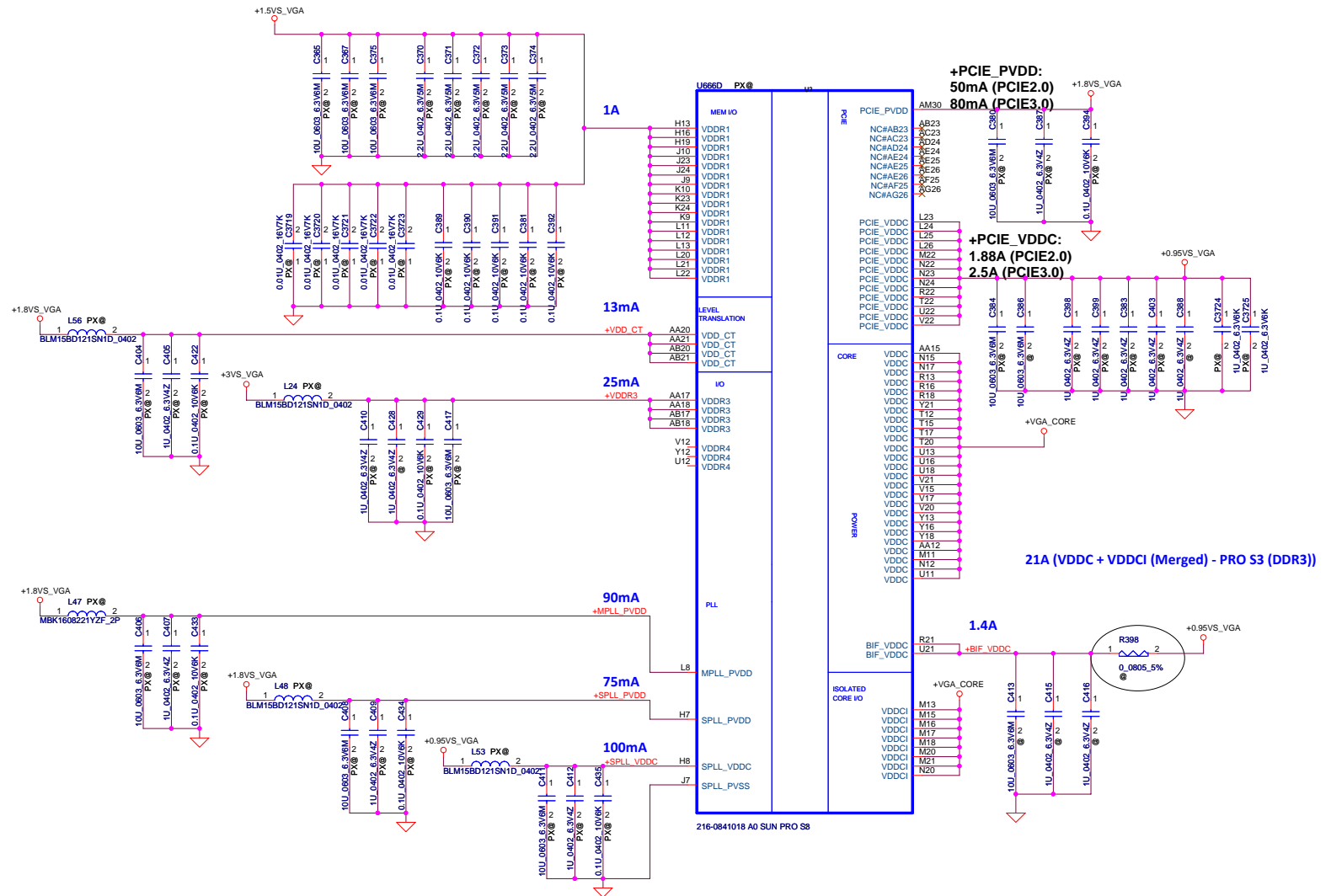
Memory ID	Memory Type	Configuration	Size	R5174	R5169	X76 P/N
000	SA000068U00	Samsung K4W2G1646E-BC1A	1GB	NC	4.75K	X7654132L01
001	SA000067500	Micron MT41J128M16JT-093G:K	1GB	8.45K	2K	X7654132L03
010	SA00006H400	Hynix H5TC2G63FRR-11C	1GB	4.53K	2K	X7654132L02
011	SA000076P00	Samsung K4W4G1646D-BC1A	2GB	6.98K	4.99K	X7654132L04
100	SA000077K00	Micron MT41J256M16HA-093G:E	2GB	4.53K	4.99K	X7654132L05
101	SA00006E800	Hynix H5TC4G63AFRR-11C	2GB	3.24K	5.62K	X7654132L14
110	SA000068U40	Samsung K4W2G1646Q-BC1A	1GB	3.4K	10K	X7654132L13

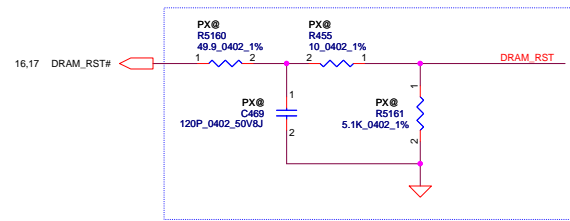
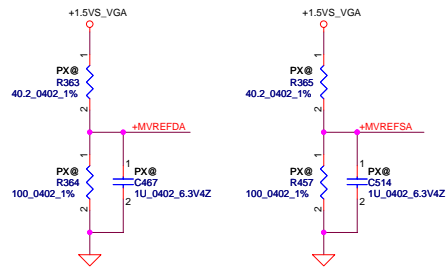
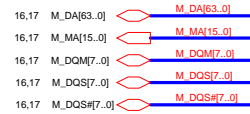


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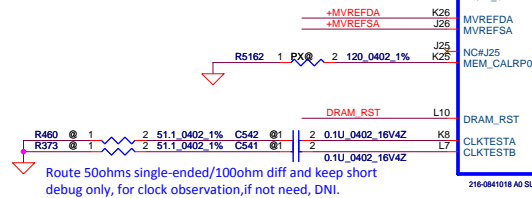


+3VS_VGA	10uF	1uF	0.1uF
VDDR3 25mA	0	2 (1@)	1

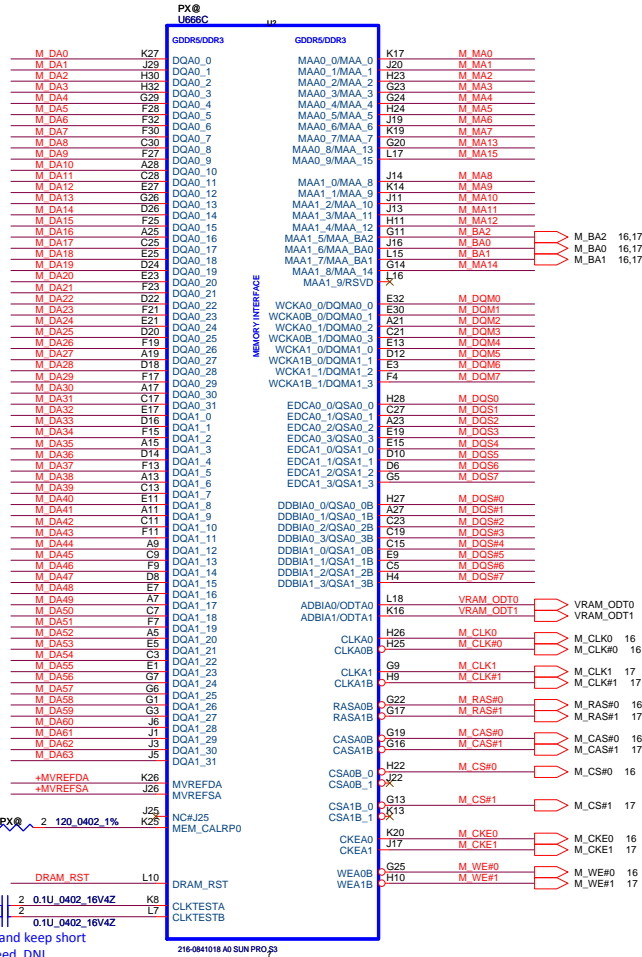




Place close to GPU (within 25mm)
and place component close to each other

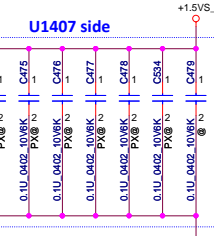
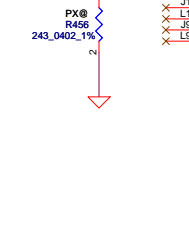
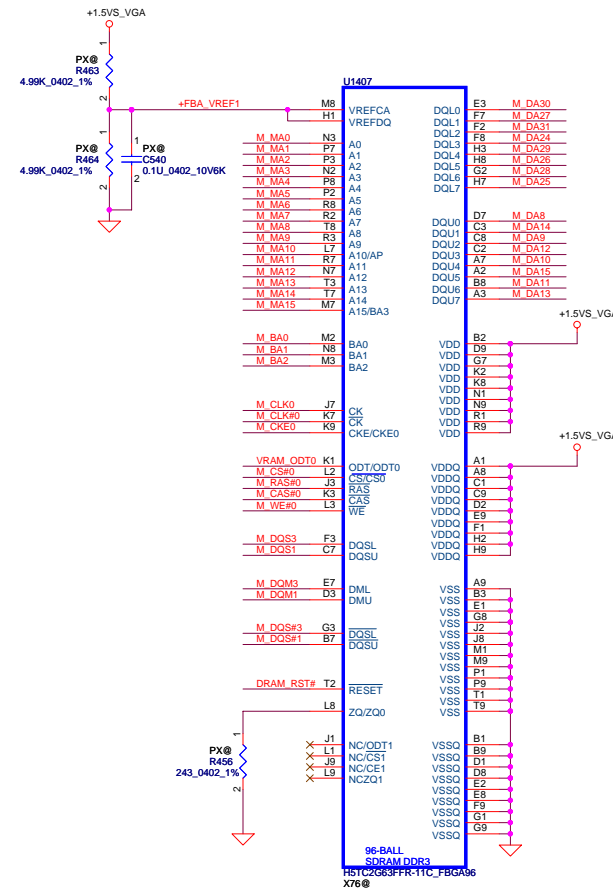
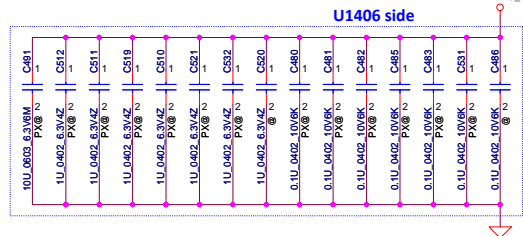
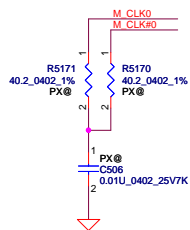
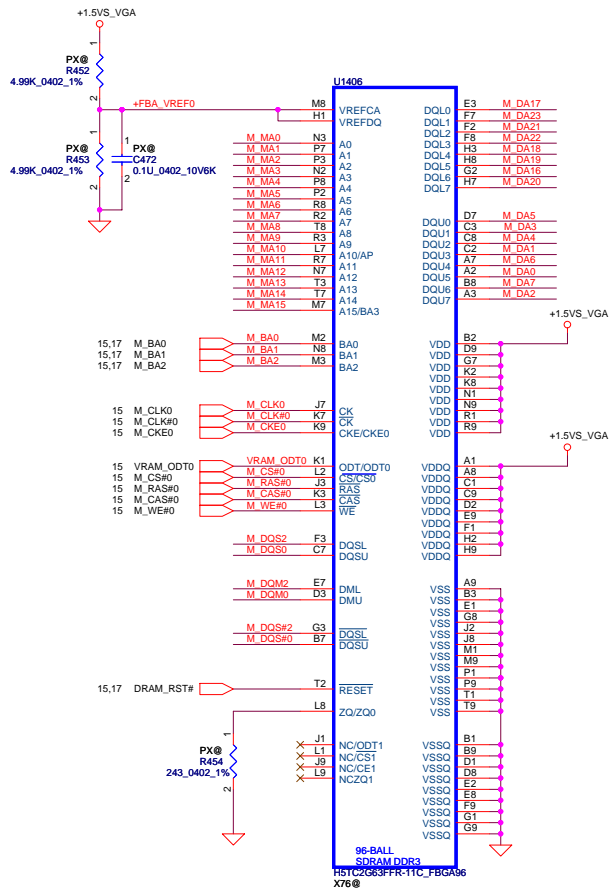


Route 50ohms single-ended/100ohm diff and keep short
debug only, for clock observation, if not need, DNI.



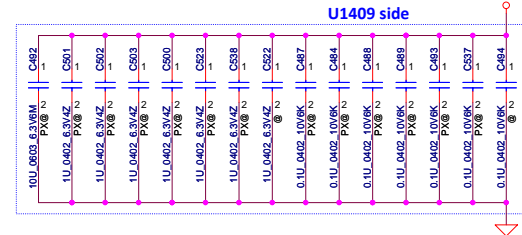
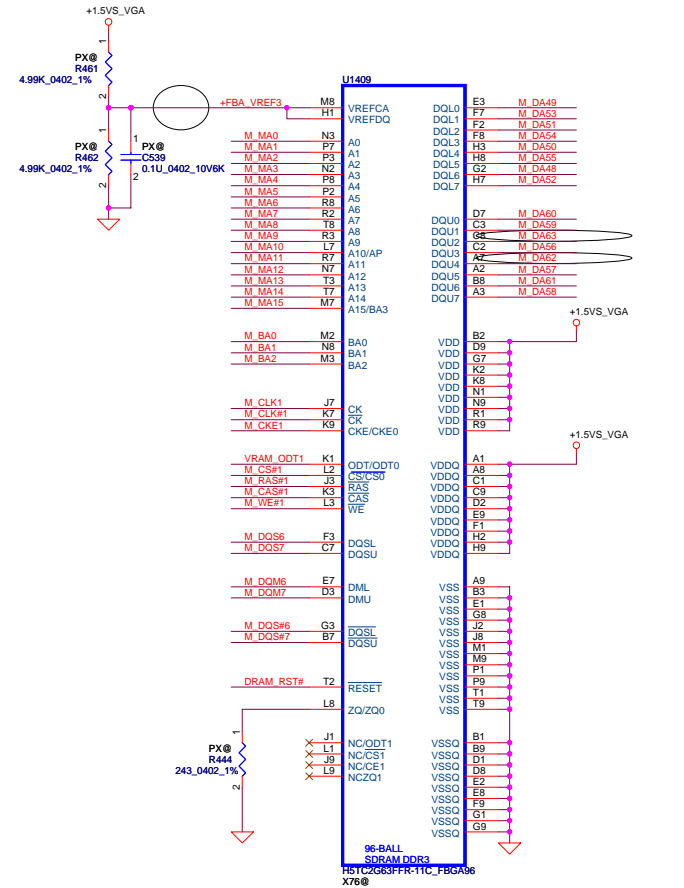
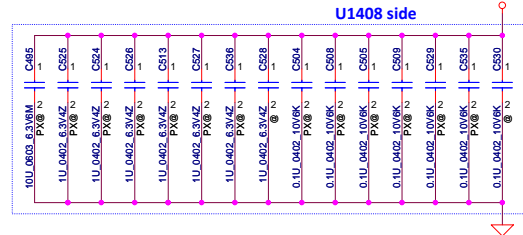
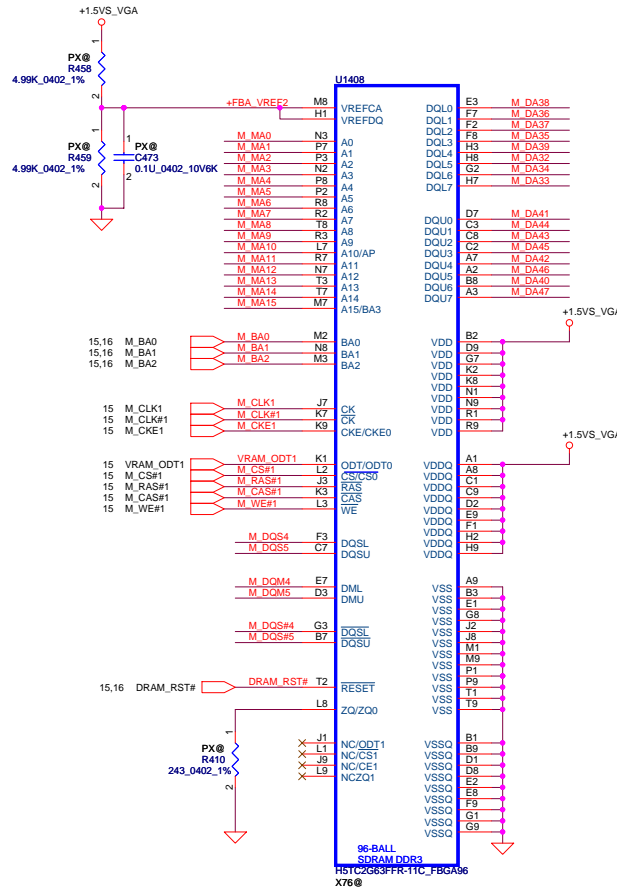
Memory Partition A - Lower 32 bits

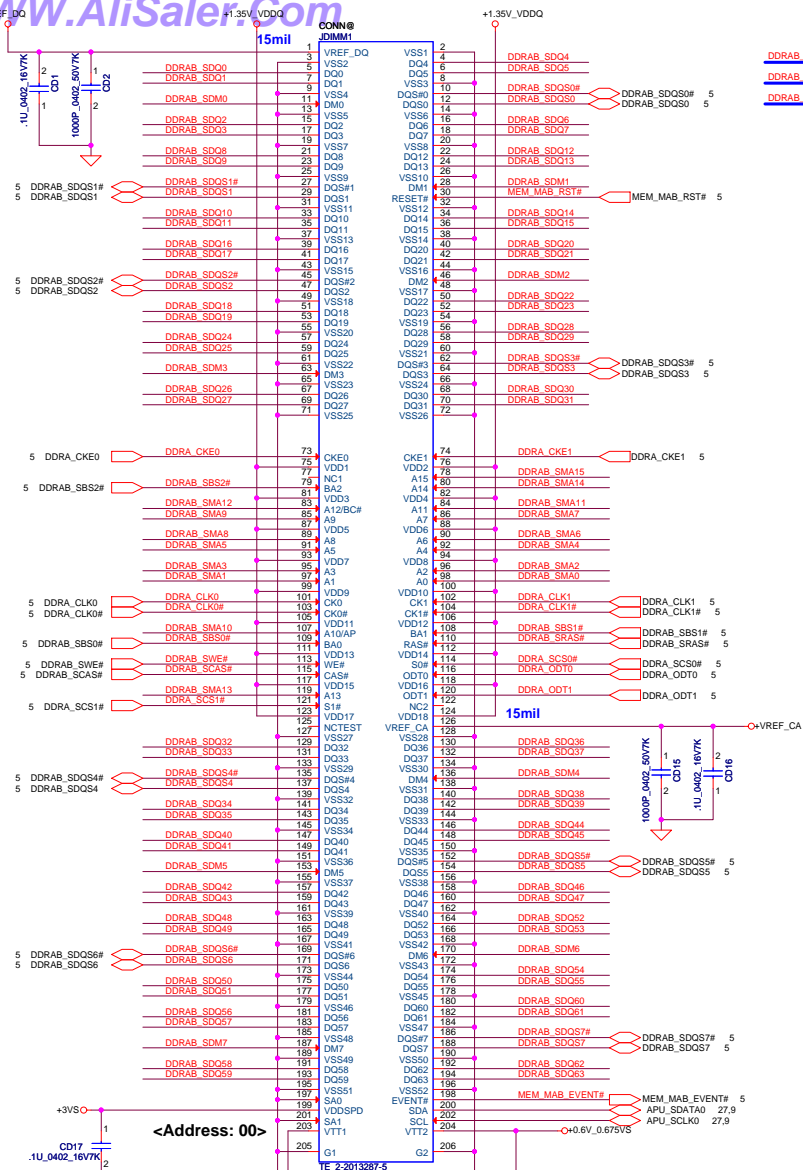
15,17 M_DA[63..0] M_DA[63..0]
 15,17 M_MA[15..0] M_MA[15..0]
 15,17 M_DQM[7..0] M_DQM[7..0]
 15,17 M_DQS[7..0] M_DQS[7..0]
 15,17 M_DQS#[7..0] M_DQS#[7..0]



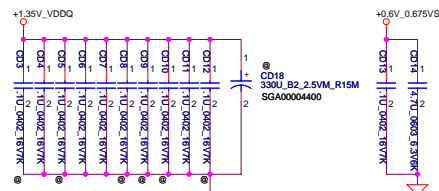
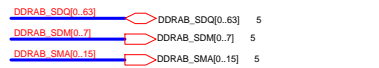
Memory Partition A - Upper 32 bits

15,16 M_DA[63..0] M_DA[63..0]
 15,16 M_MA[15..0] M_MA[15..0]
 15,16 M_DQM[7..0] M_DQM[7..0]
 15,16 M_DQS[7..0] M_DQS[7..0]
 15,16 M_DQS# [7..0] M_DQS# [7..0]



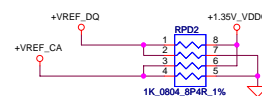


DIMM_1 H:4mm Reverse

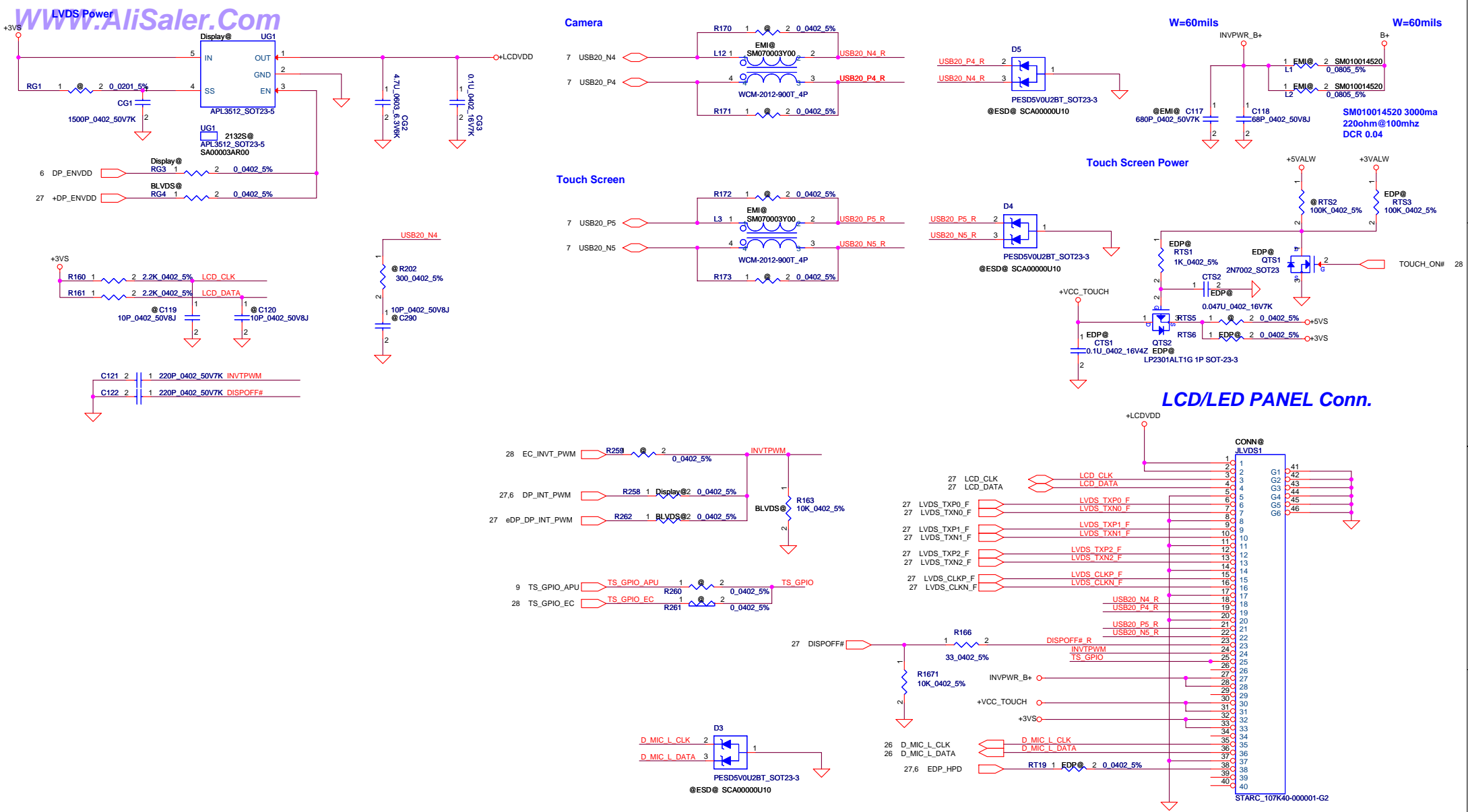


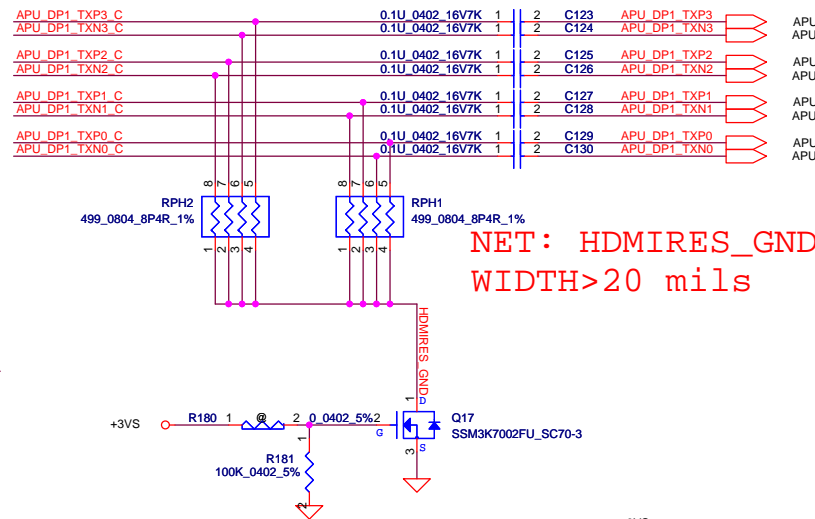
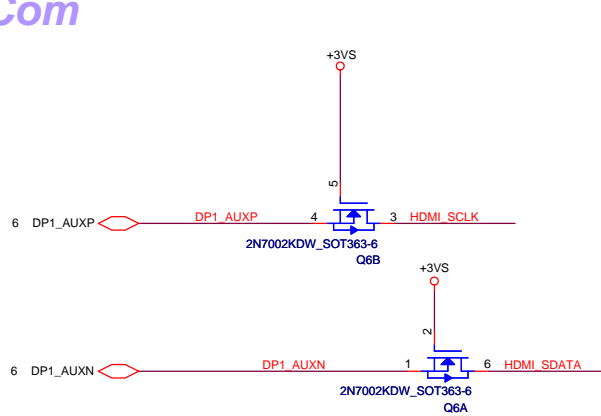
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VREF for DIMM1

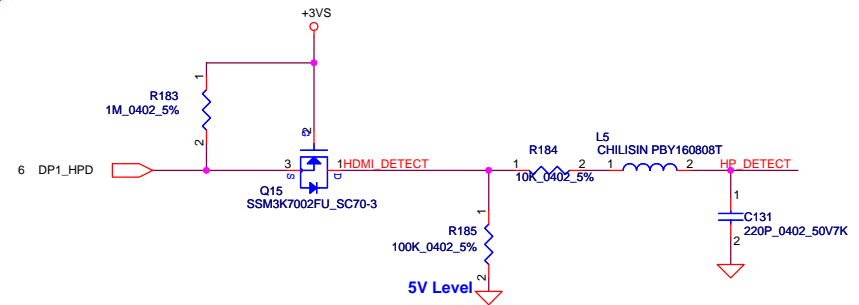
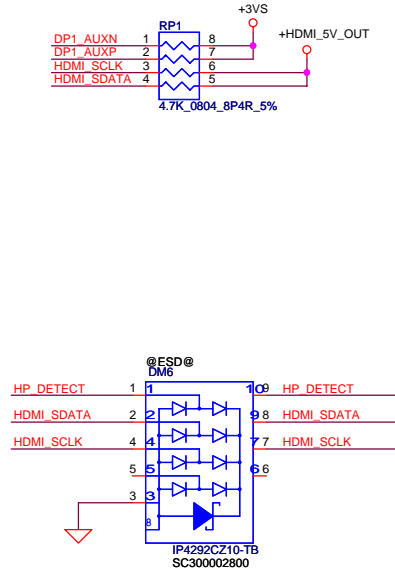
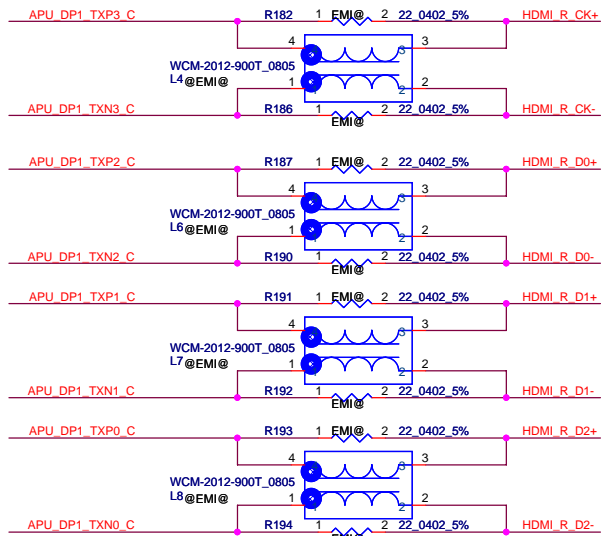


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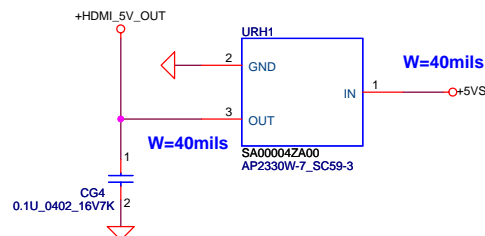
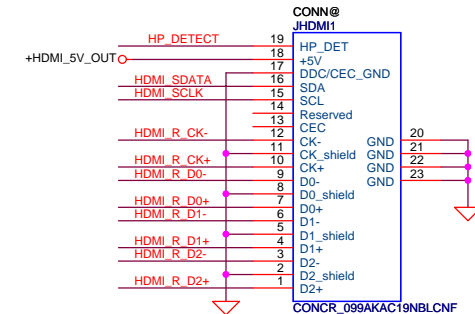




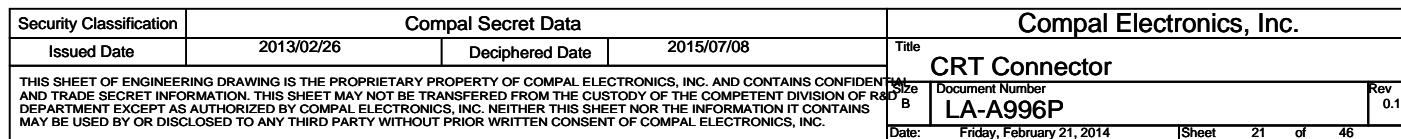
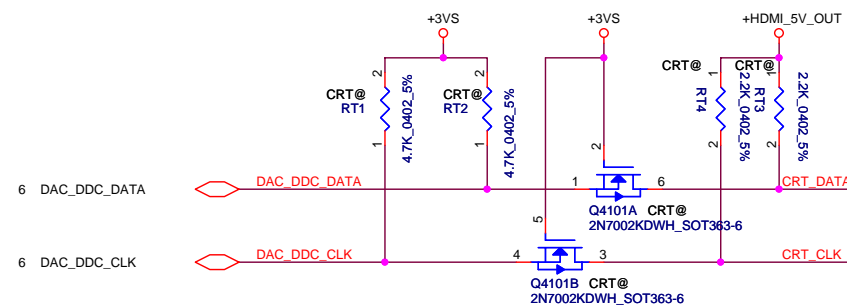
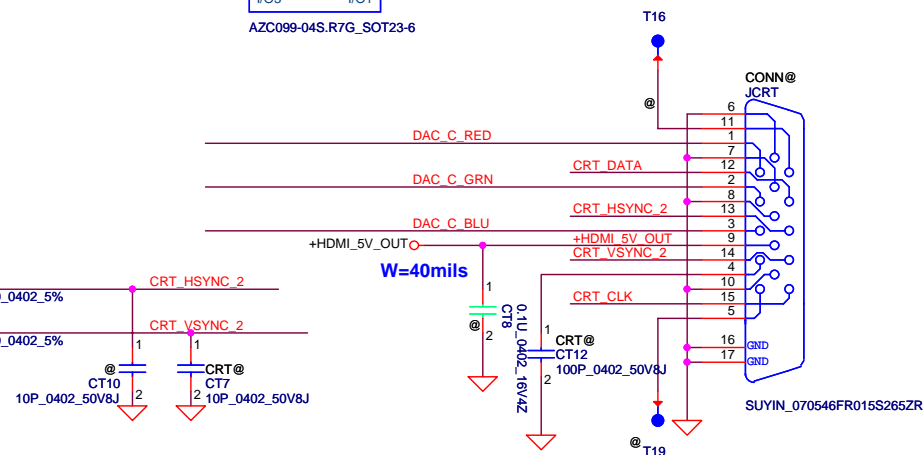
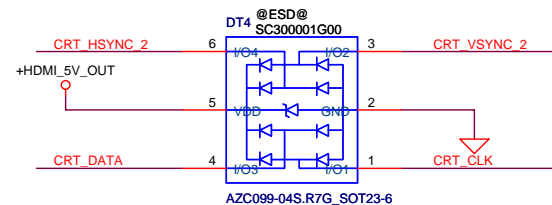
SM070001310 400ma 90ohm@100mhz DCR 0.3

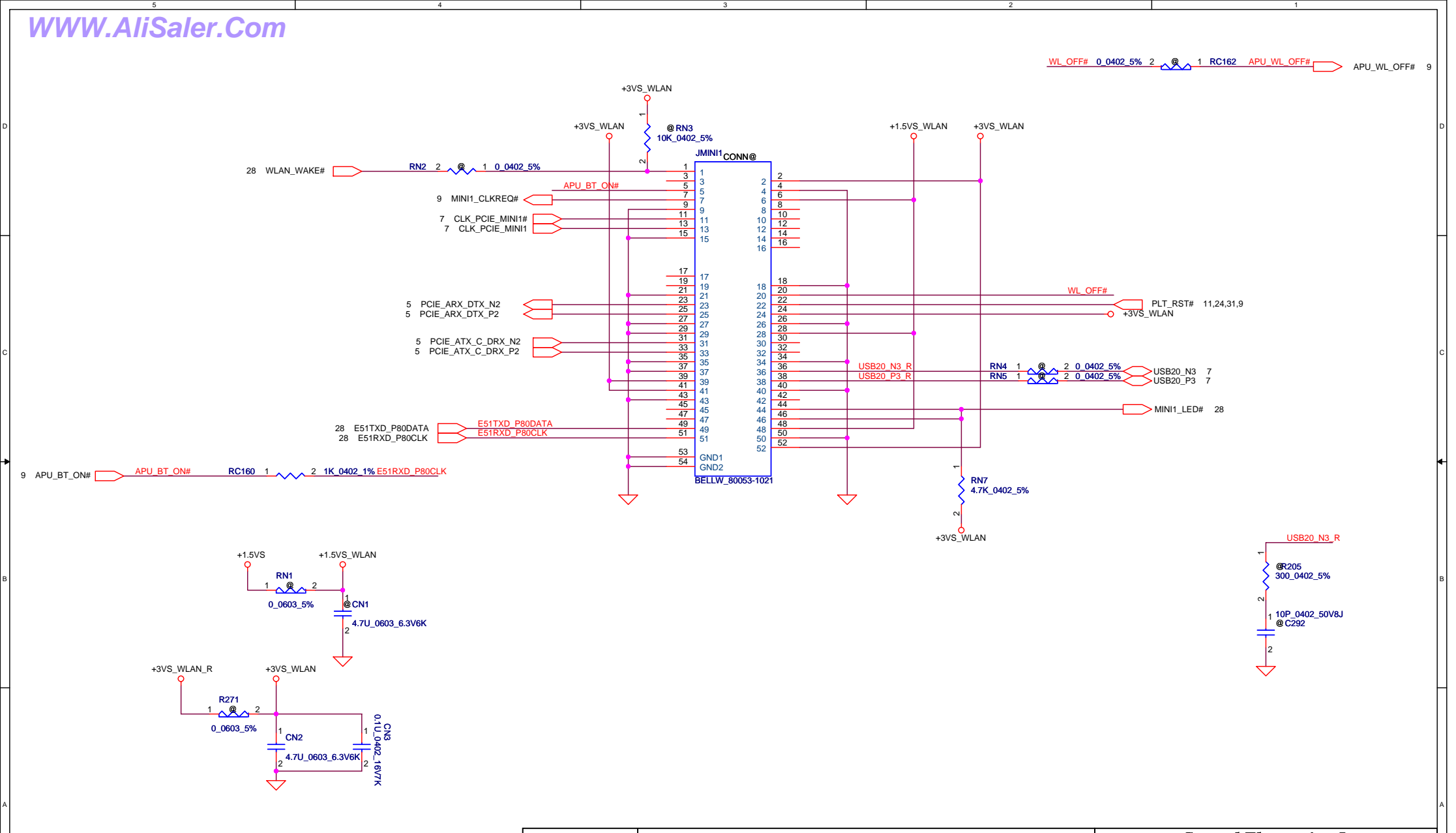


8/20 change HDMI Conn HDMI Conn.

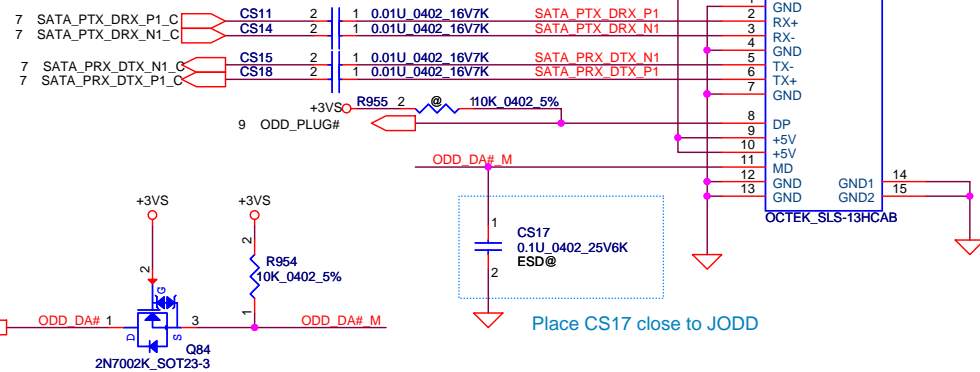
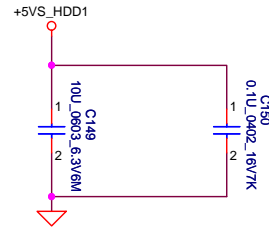


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Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	HDMI Connector		
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				Custom	LA-A996P	0.1	
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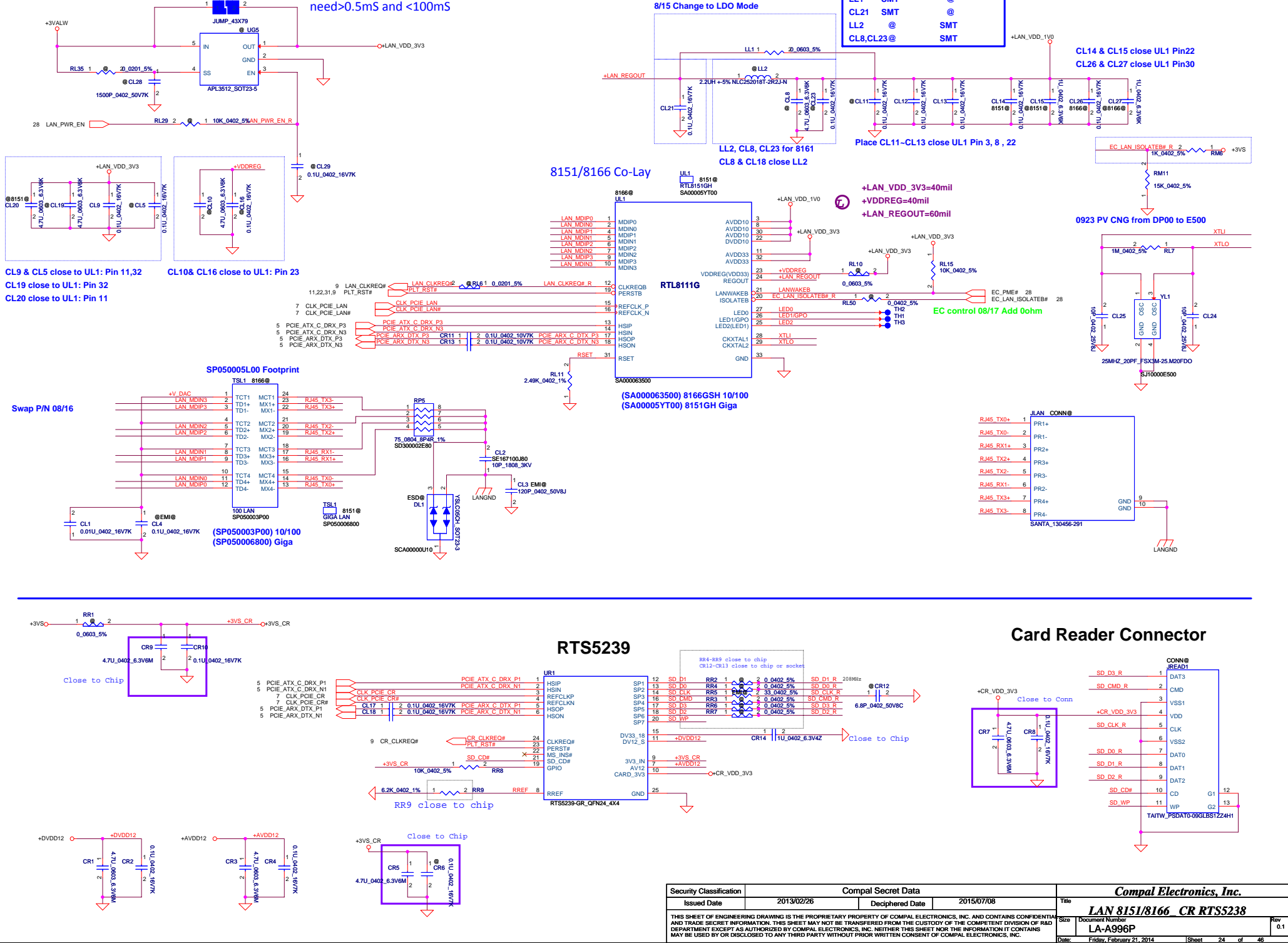


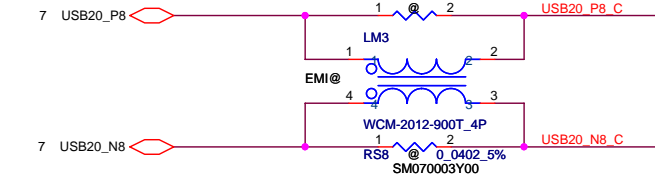
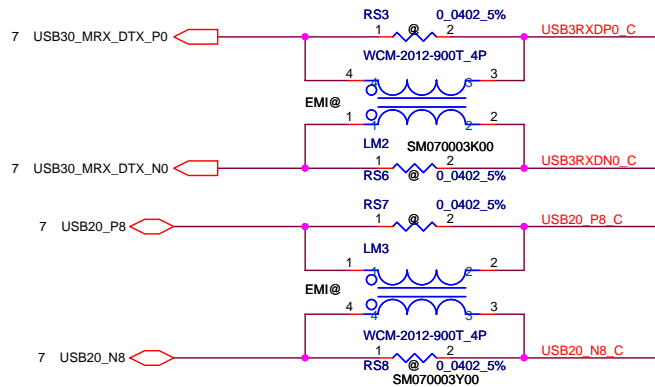
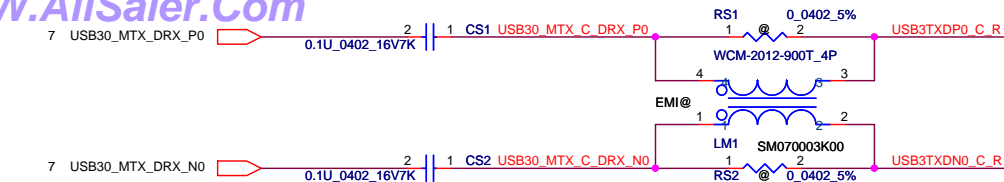
Security Classification		Compal Secret Data				Compal Electronics, Inc.					
Issued Date		2013/02/26		Deciphered Date		2015/07/08		Title			
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						Document Number				Rev	
						LA-A996P				0.1	
						Date:				Monday, February 17, 2014	



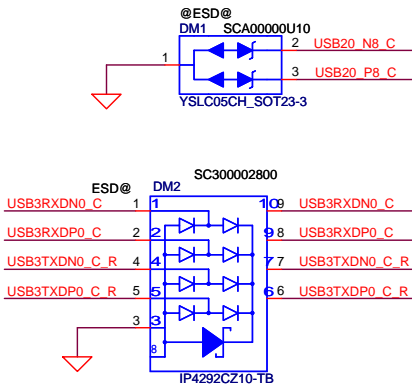
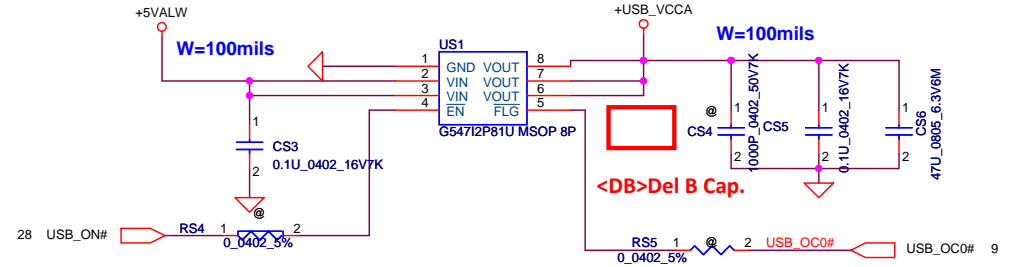
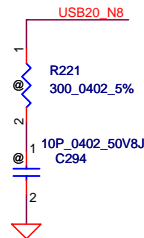
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Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	ODD/SATA Conn
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				LA-A996P	0.1
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+LAN_VDD_3V3 Rising time
need>0.5ms and <100ms

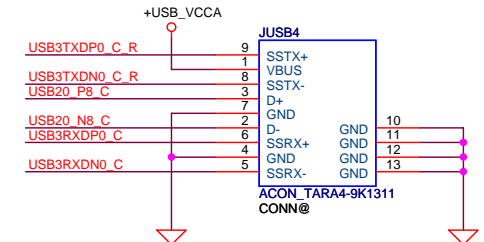




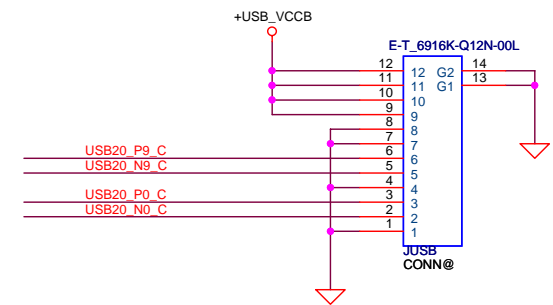
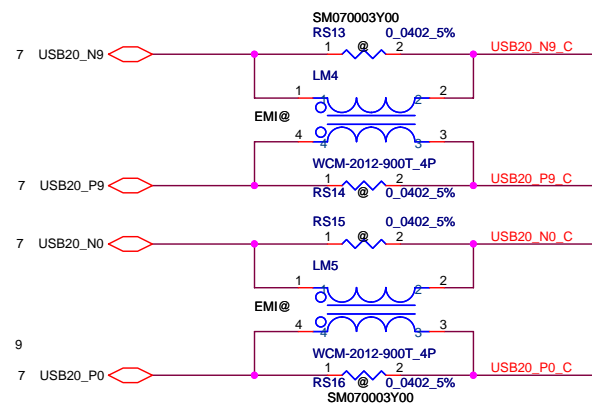
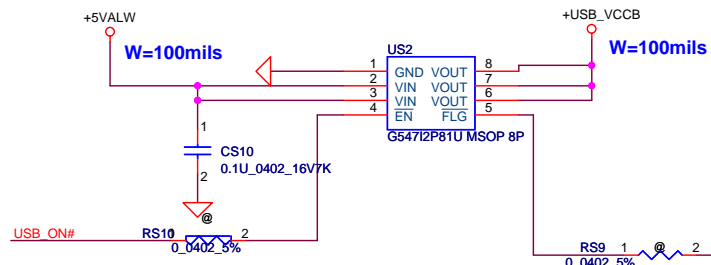
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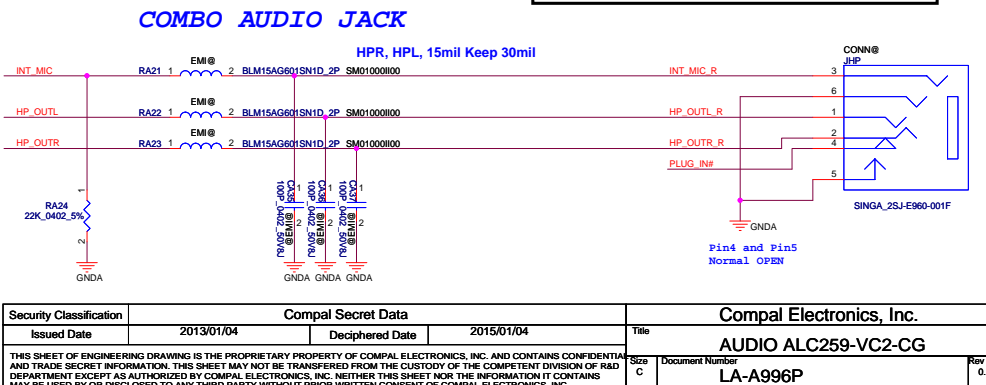
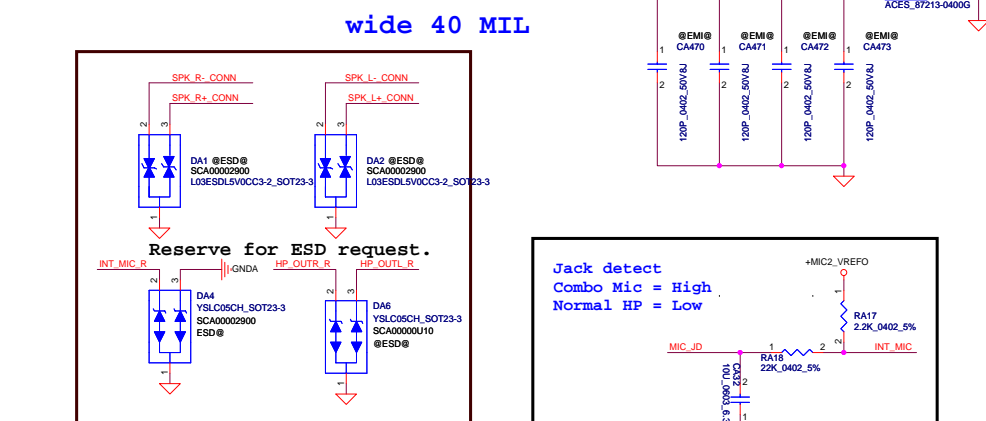
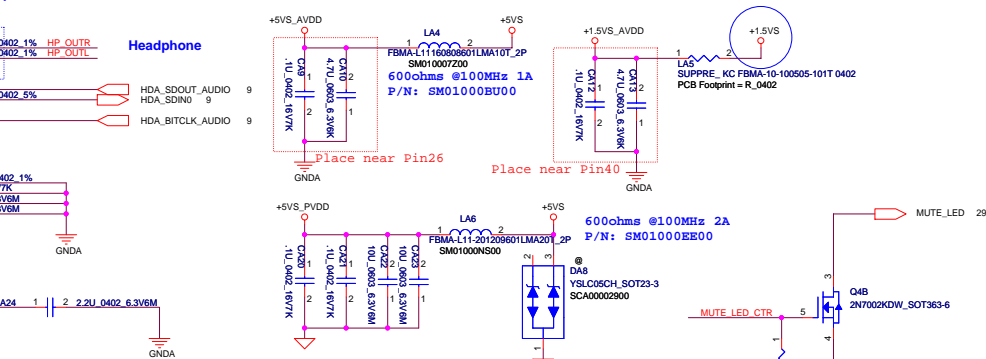
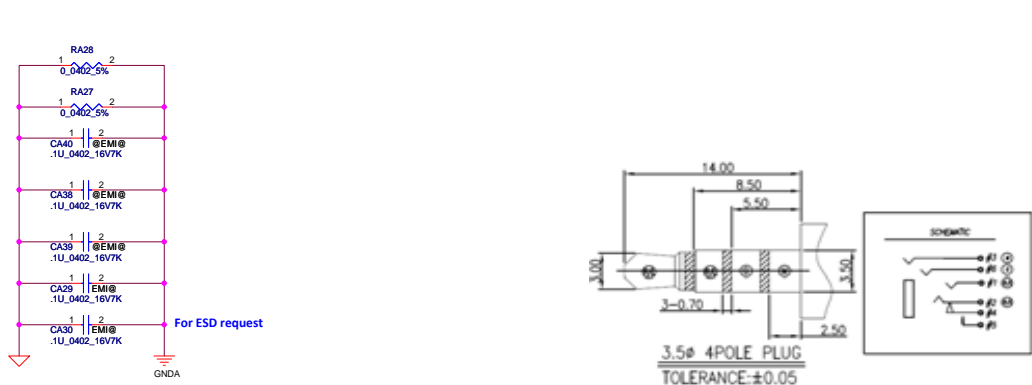
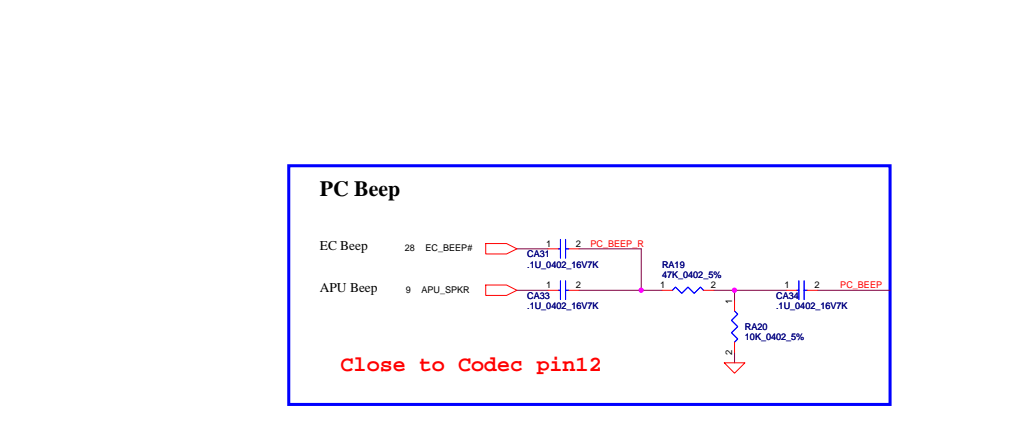
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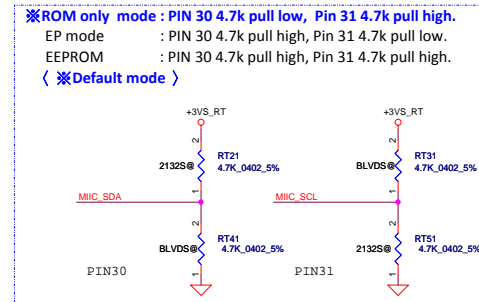
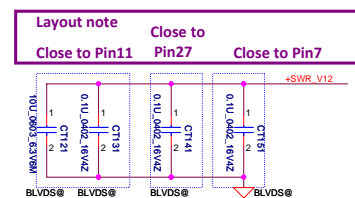
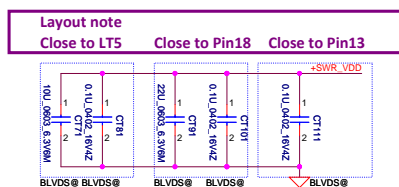
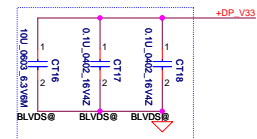


USB2.0 port x 2



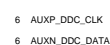
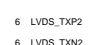
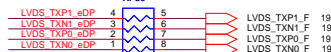
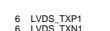
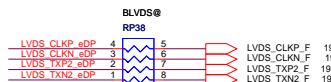
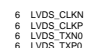
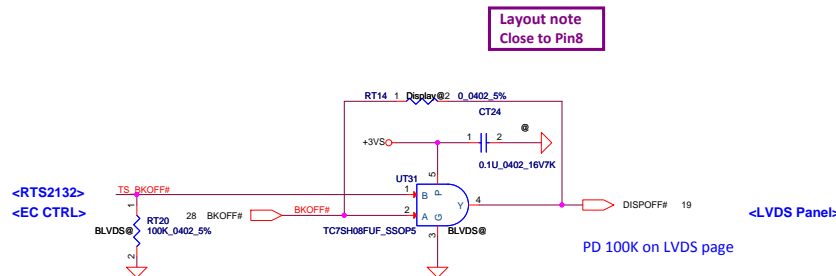
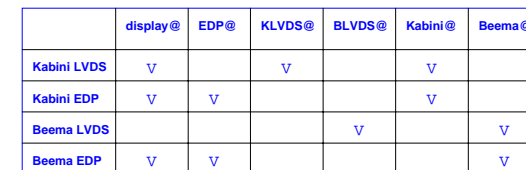
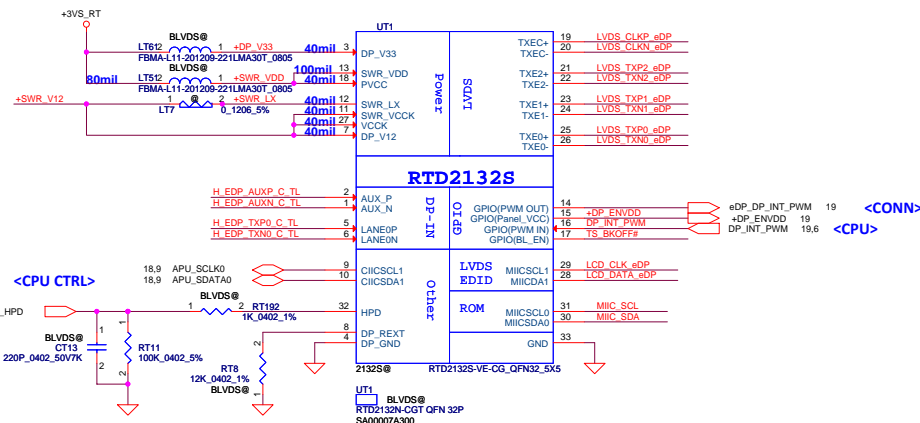
Security Classification		Compal Secret Data		Title	
Issued Date	2013/02/26	Deciphered Date	2015/07/08	USB 3.0/2.0 conn	
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				LA-A996P	0.1
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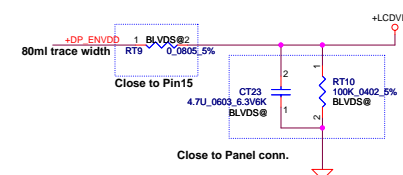
SWR / LDO Mode select		
	LDO	SWR
2132S	Do not support	mount LT7
2132N	Use 0 ohm	mount LT7

※ If use 2132N, please select LDO mode as default.



RP40 Close CPU				RT24~27 Close JLVDS conn				
LVDS TXP2	RT33	Display@2	0.0402 %	LVDS TXP2 K	RT24	KLVDS@2	0.0402 %	LVDS TXP2 F
LVDS TXN2	RT36	Display@2	0.0402 %	LVDS TXN2 X	RT25	KLVDS@2	0.0402 %	LVDS TXN2 F
AUXN DDC CLK	RT35	Display@2	0.0402 %	AUXN DDC CLK K	RT26	KLVDS@2	0.0402 %	AUXN DDC CLK F
AUXN DDC DATA	RT34	Display@2	0.0402 %	AUXN DDC DATA K	RT27	KLVDS@2	0.0402 %	LCD CLK

Security Classification	Compal Secret Data	<i>Compal Electronics, Inc.</i>
Issued Date	2013/02/26 Deciphered Date 2015/07/08	eDP to LVDS
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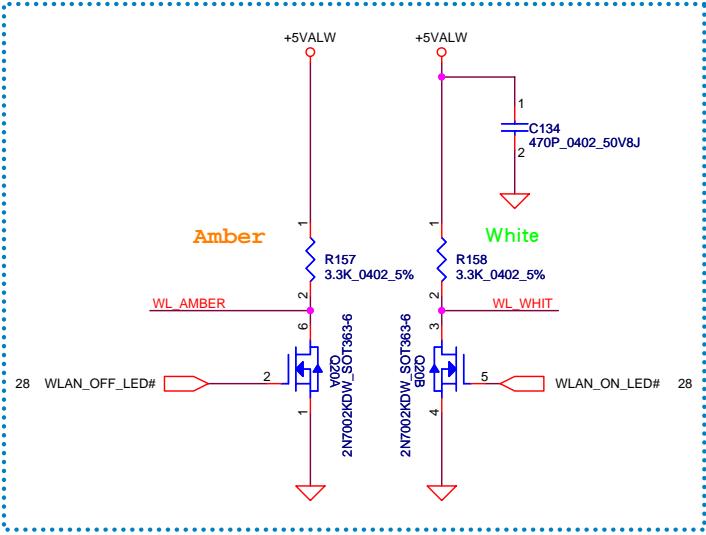
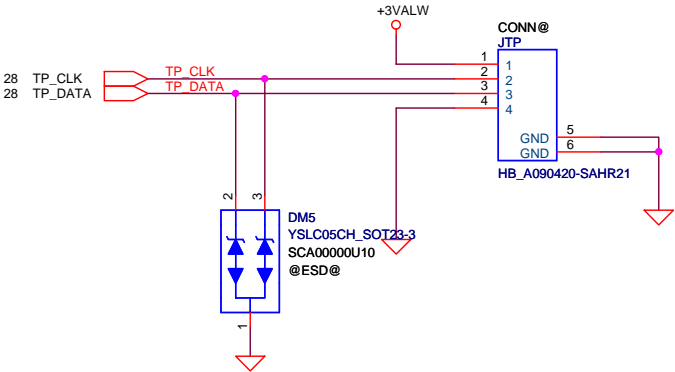


<i>15"</i>	<i>DB</i>	<i>SI</i>	<i>PV</i>	<i>MV</i>
<i>UMA R214</i>	<i>12k ohm</i>	<i>20K ohm</i>	<i>33K ohm</i>	<i>56K ohm</i>
<i>DIS R214</i>	<i>160k ohm</i>	<i>240k ohm</i>	<i>330k ohm</i>	<i>560k ohm</i>

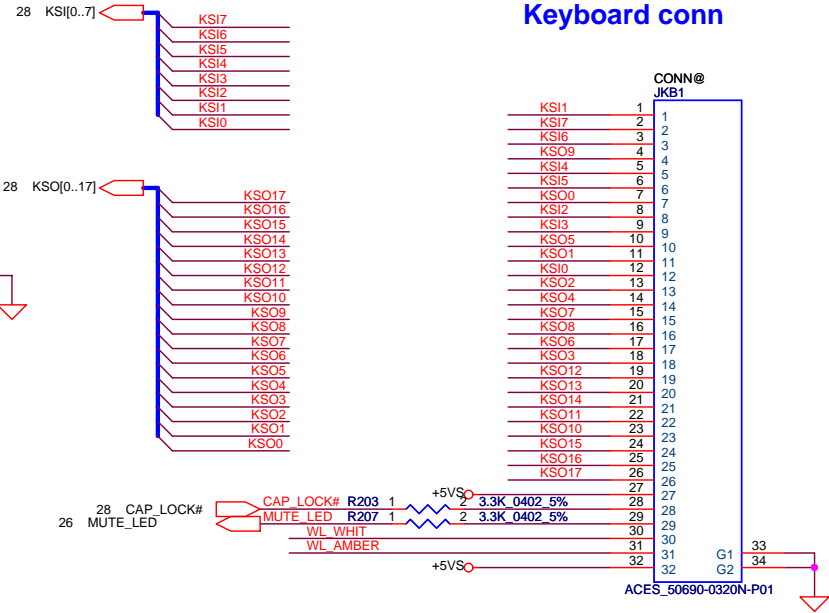
	<i>PANEL_SELECTION</i>
<i>LVDS</i>	<i>0</i>
<i>eDP</i>	<i>1</i>

Security Classification		Compal Secret Data		Compal Electronics, Inc.				
Issued Date	2011/07/08	Deciphered Date	2015/07/08	Title				
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				Size	C	Document Number	LA-A996P	
				Issue	Wednesday, August 26, 2014	Sheet	28	of

Touch pad conn

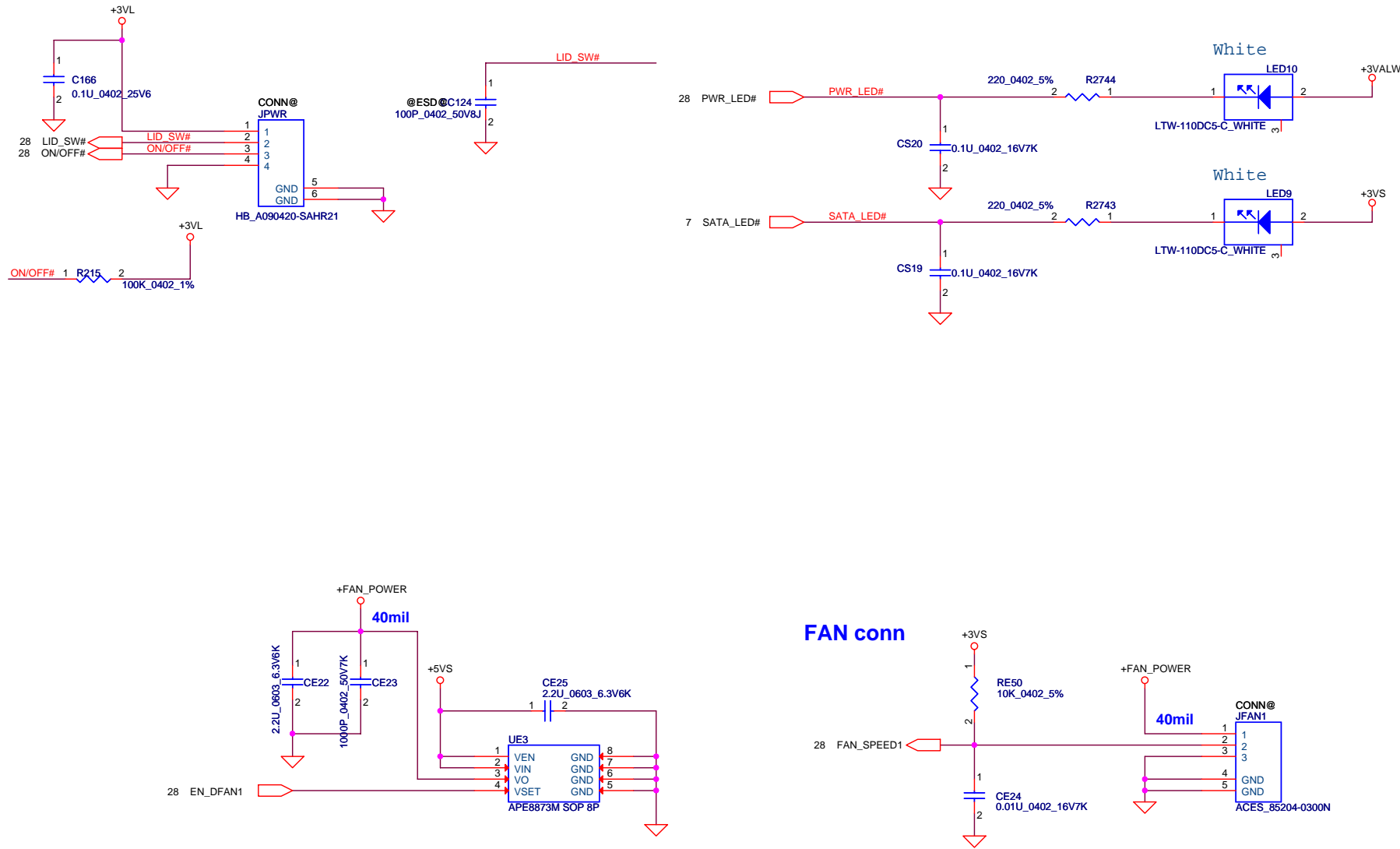


Keyboard conn

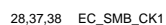


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Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	KB/TP
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Power Button Connector



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								PWRBTN/FAN			
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								B		LA-A996P	
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Security Classification

Compal Secret Data

Deciphered Date	2015/07/08
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	Title
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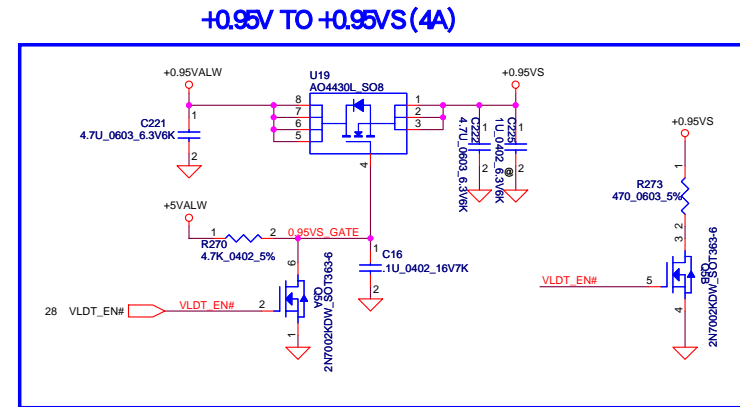
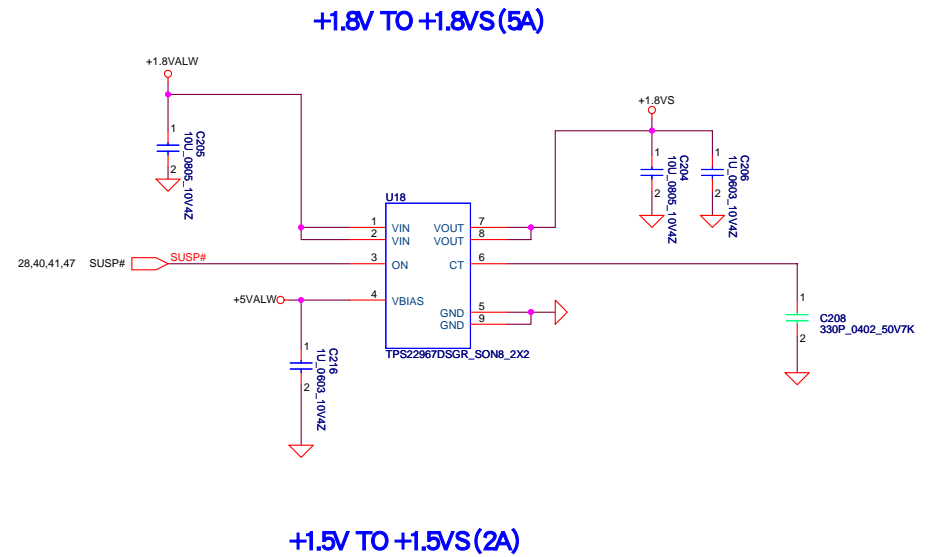
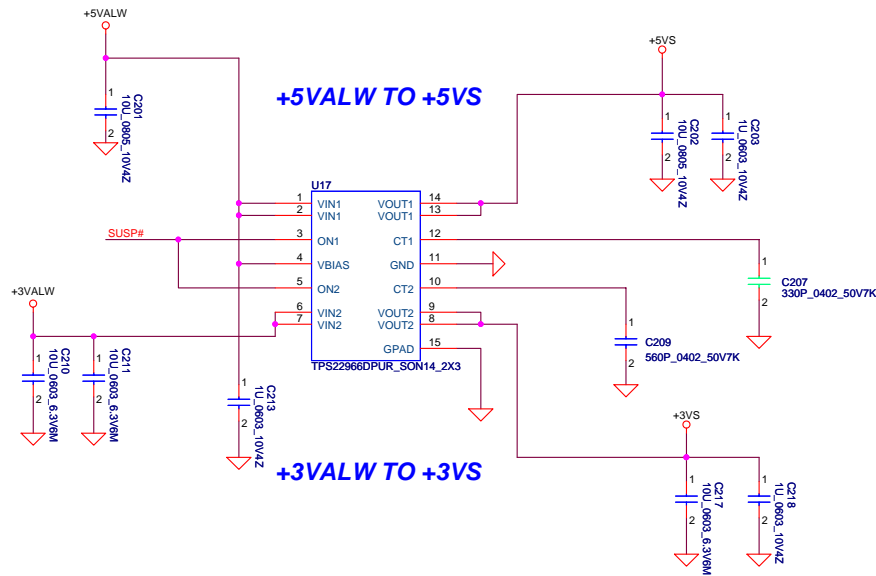
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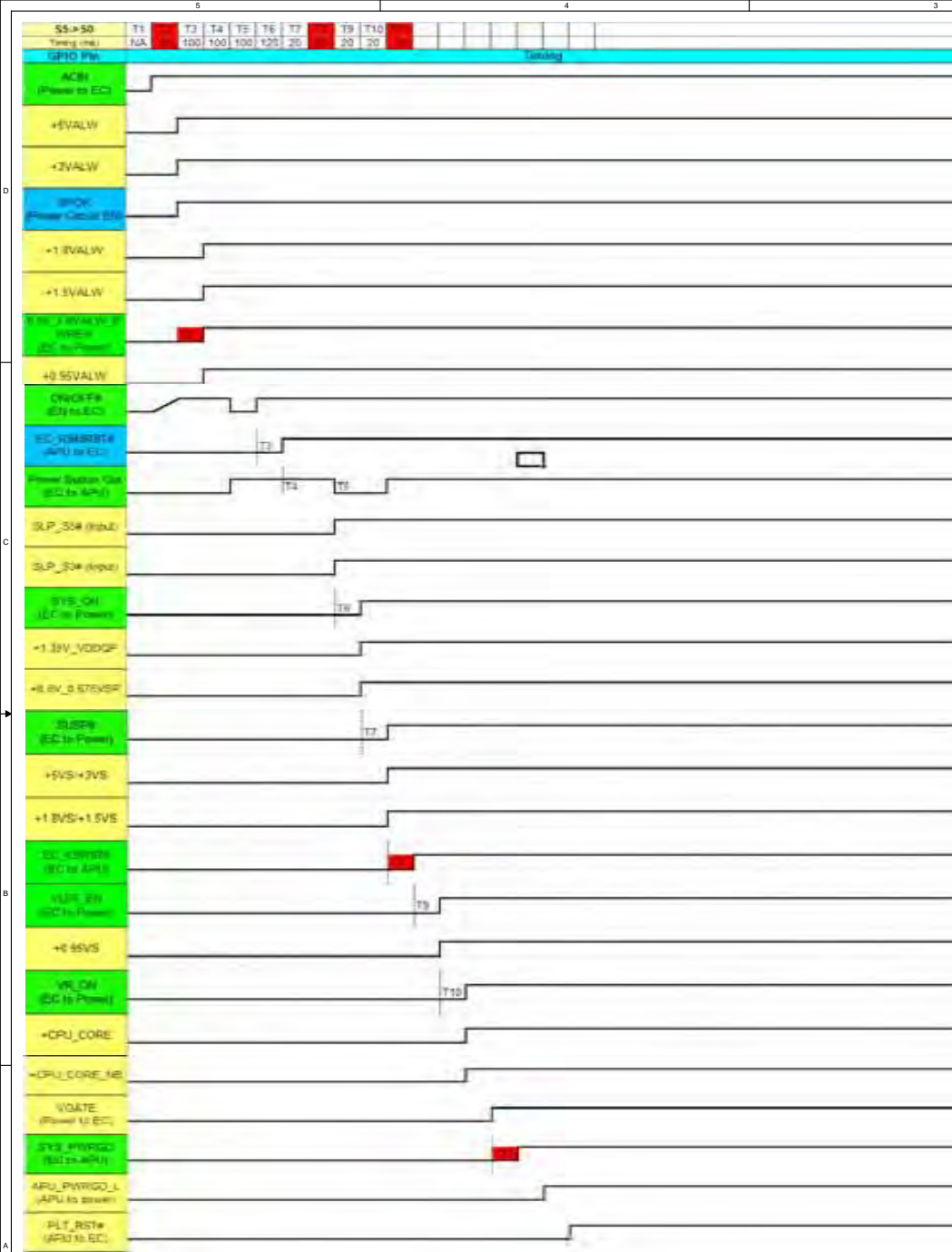
LA-A996P

Date: Monday, February 17, 2014

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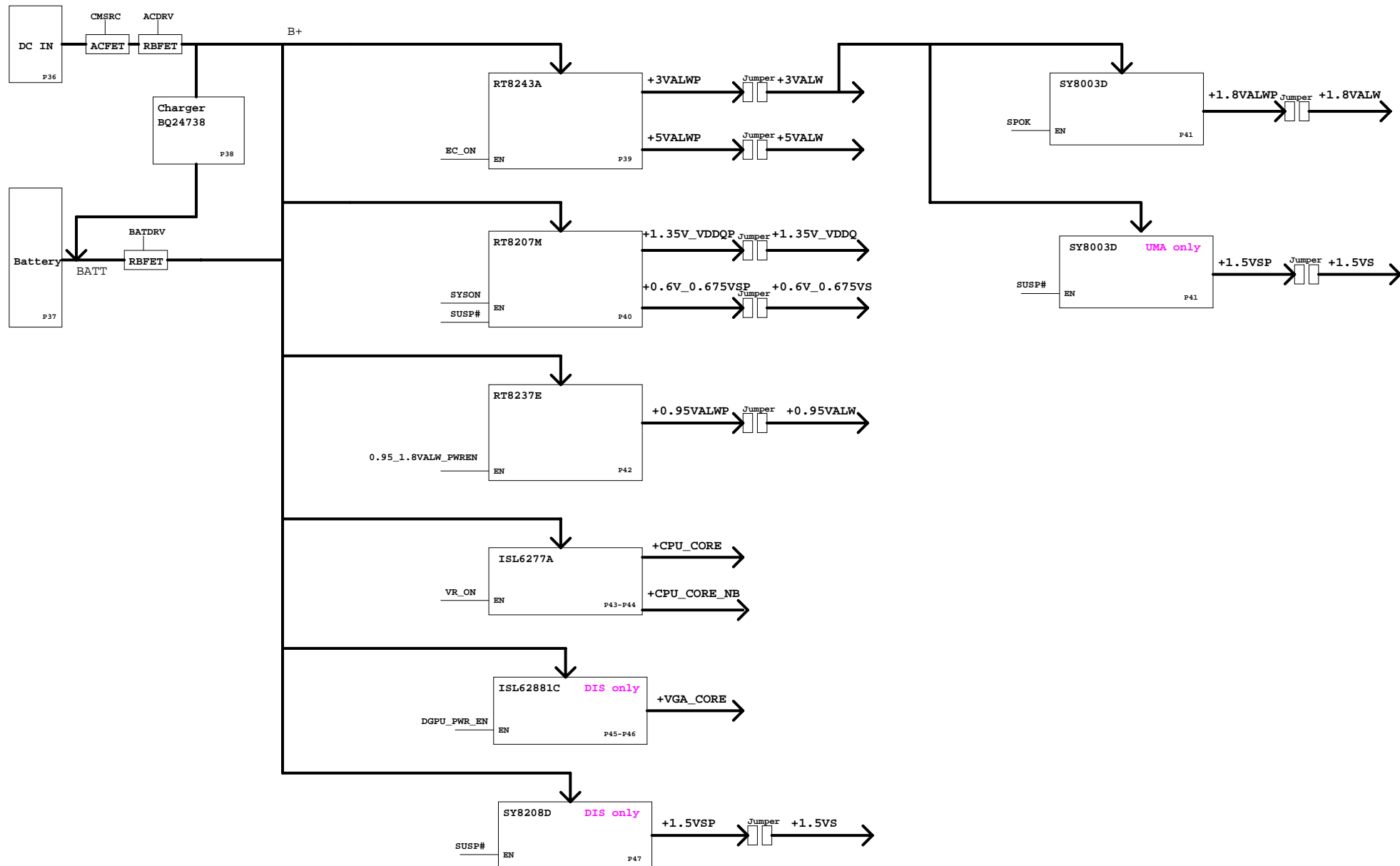




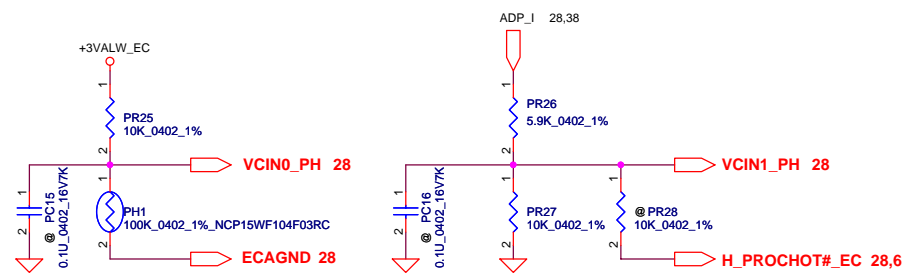
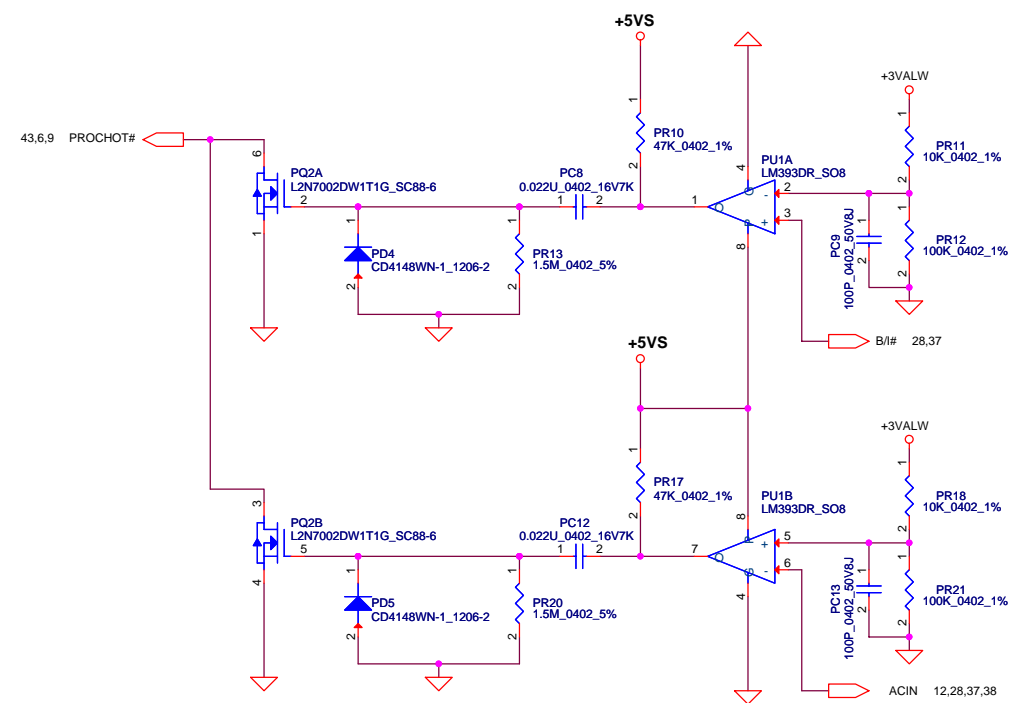
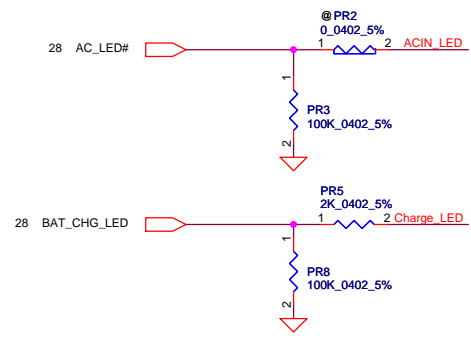
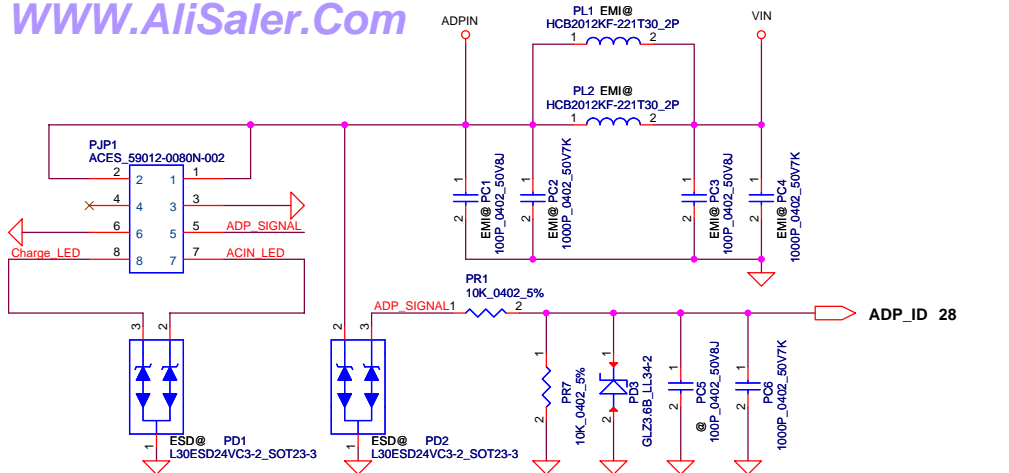
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Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	Power sequence
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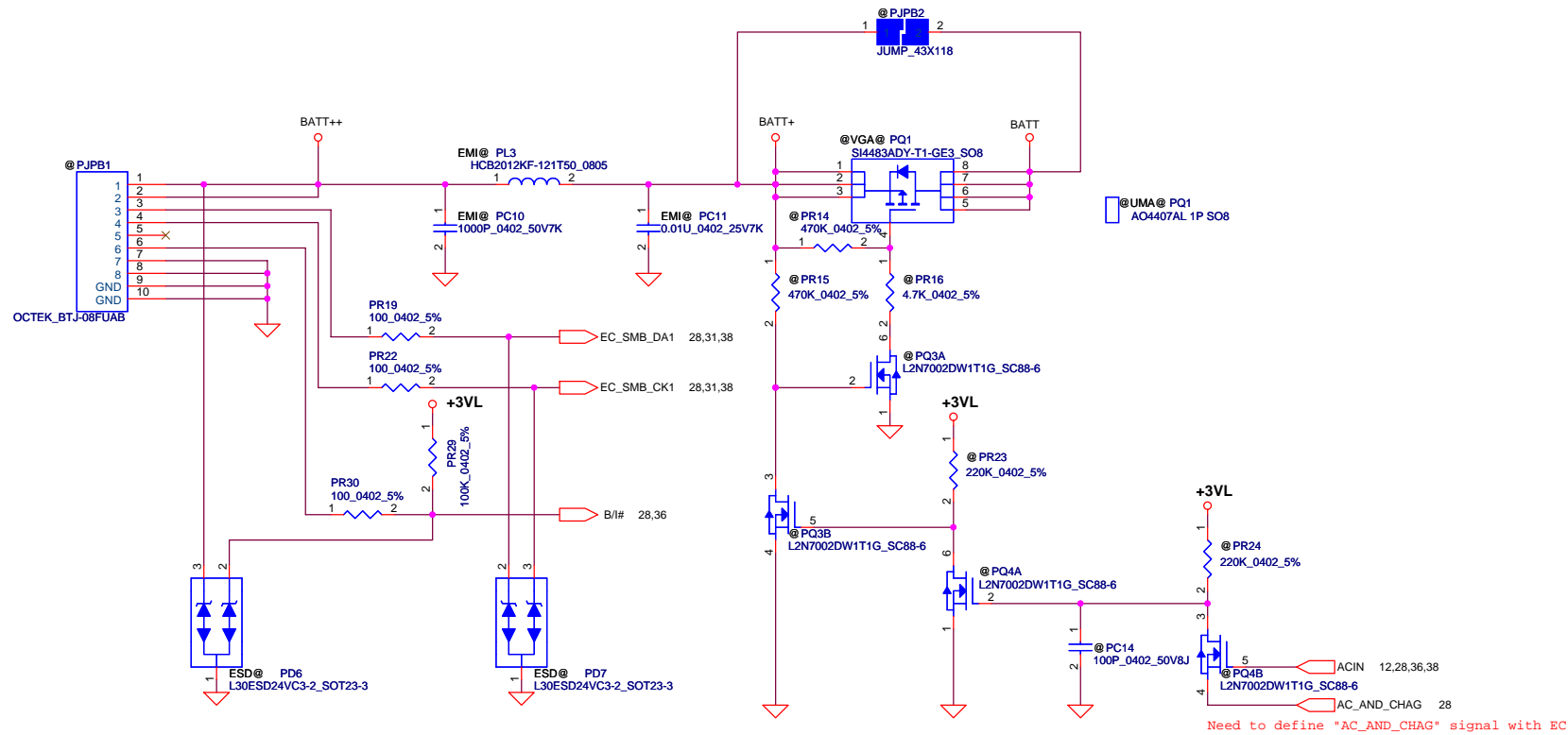
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Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	EE Change list
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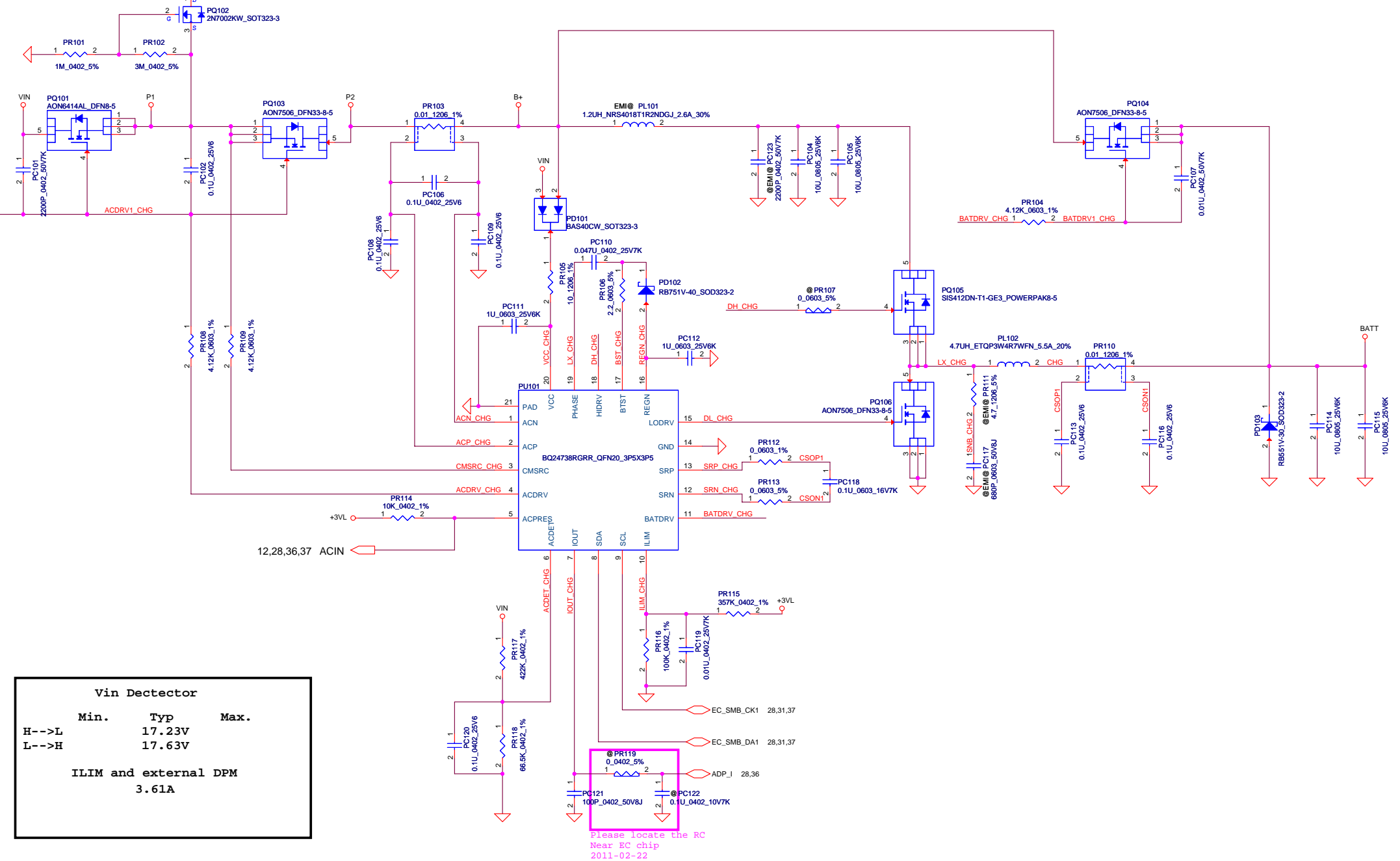
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Issued Date	2012/04/03	Deciphered Date	2014/12/31	Title	Power Block Diagram
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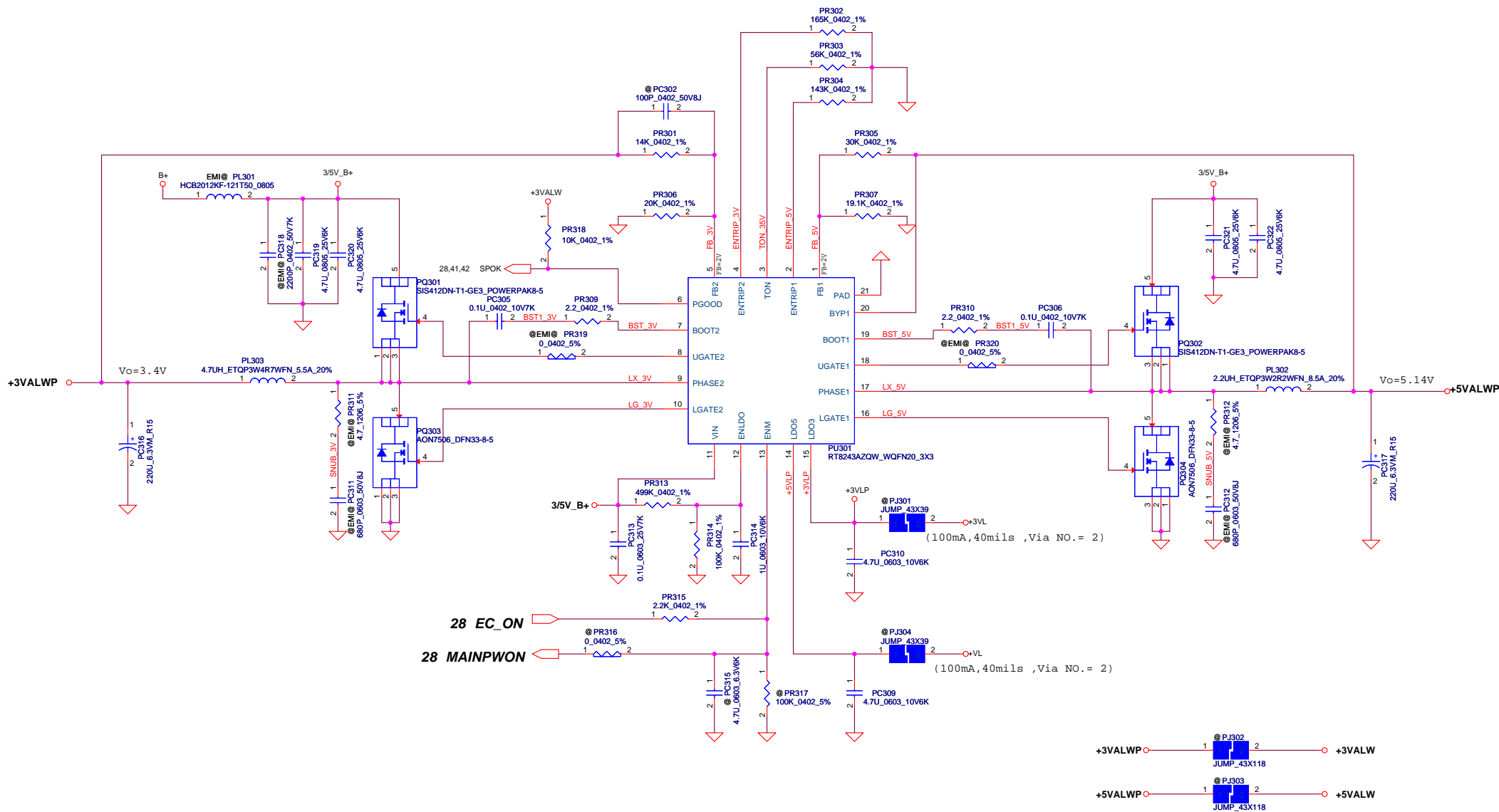


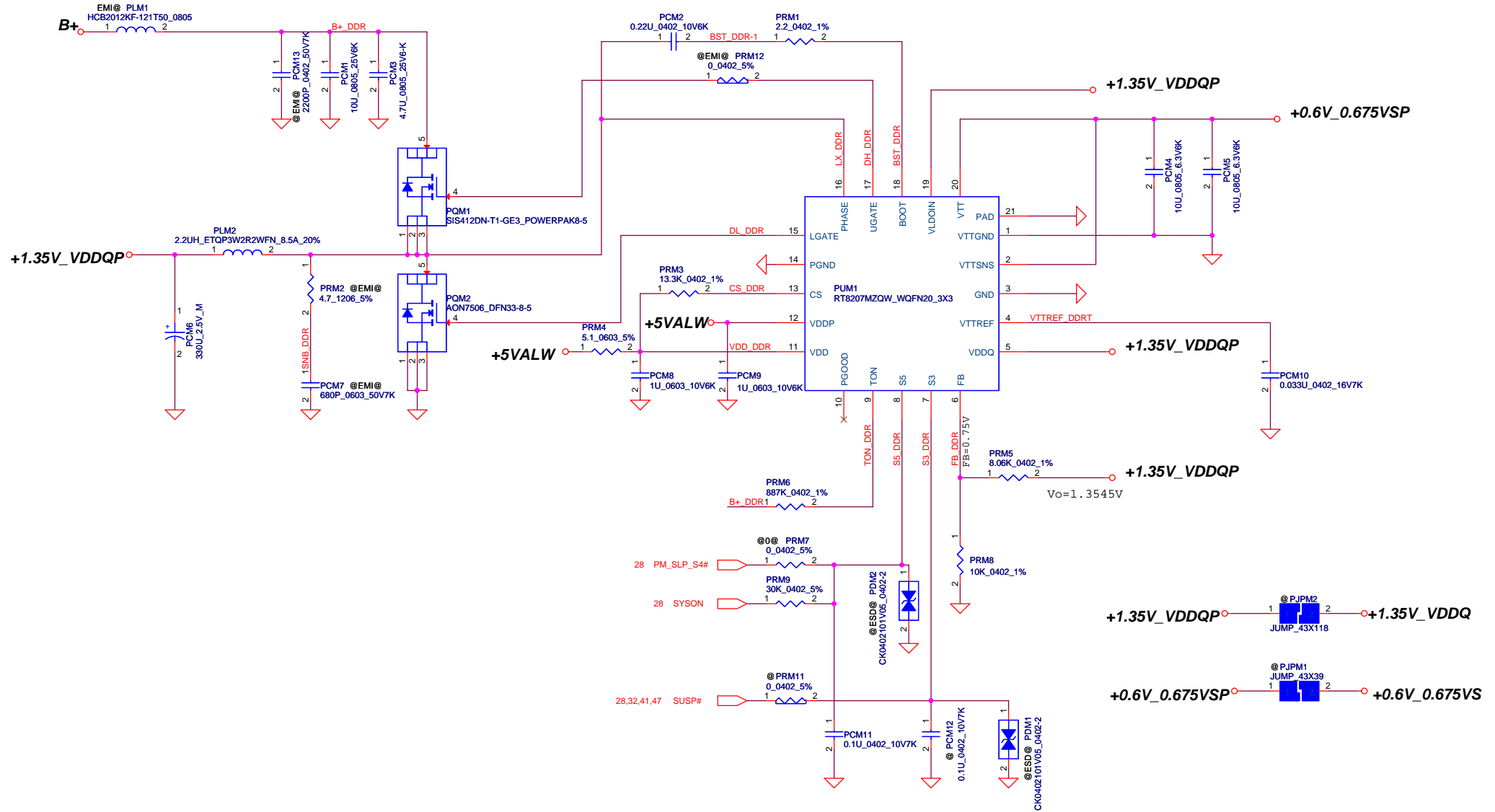
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Issued Date	2013/08/07	Deciphered Date	2016/08/06	Title	DC Conn
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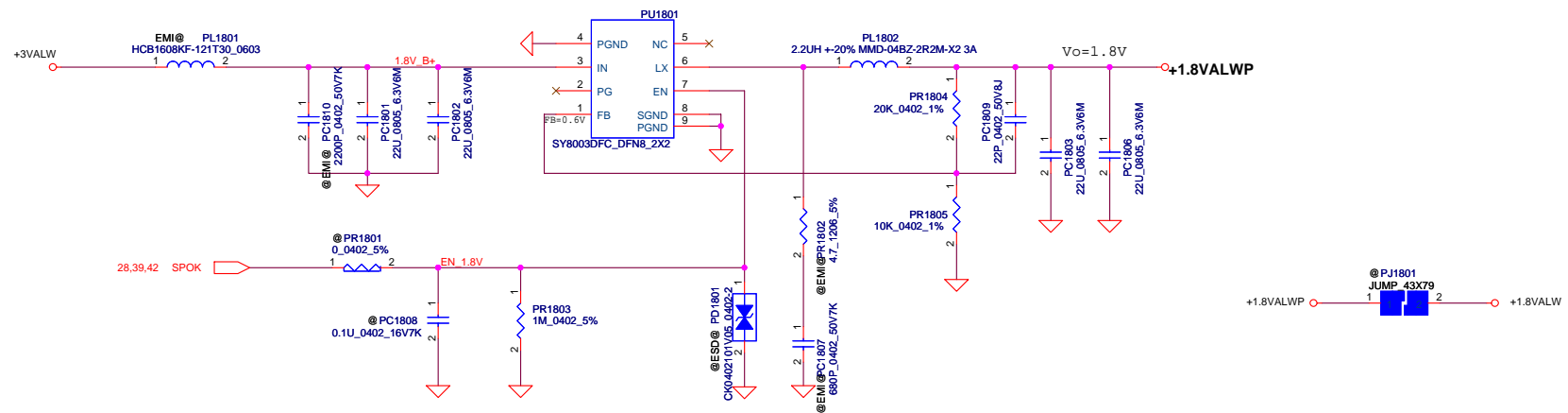
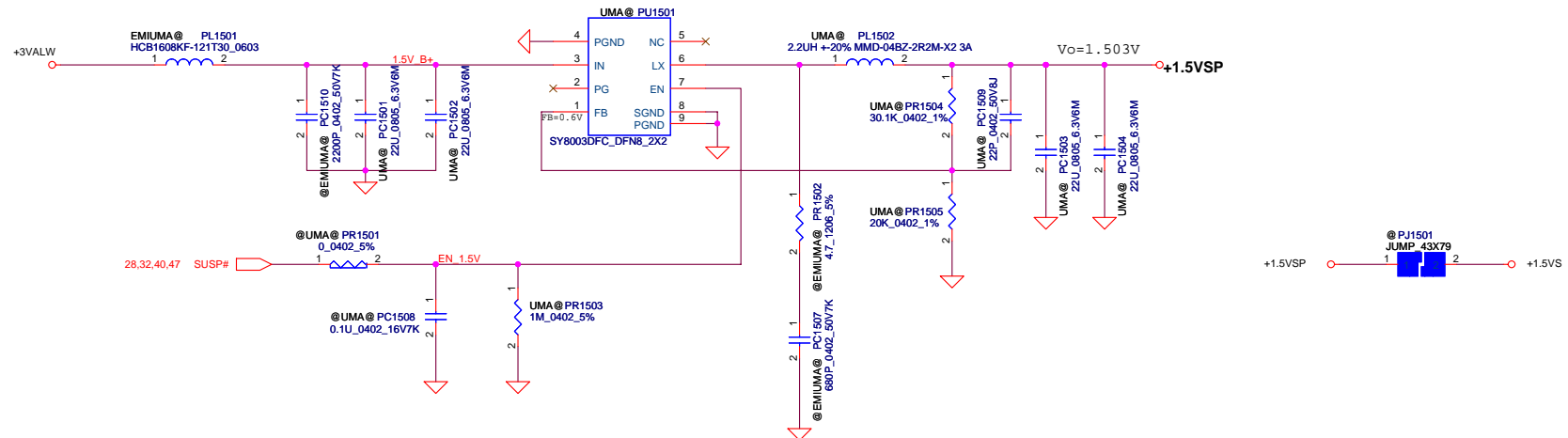
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Issued Date	2013/08/07	Deciphered Date	2016/08/06	Title	
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				Document Number	LA-A996P
				Date	Tuesday, February 25, 2014
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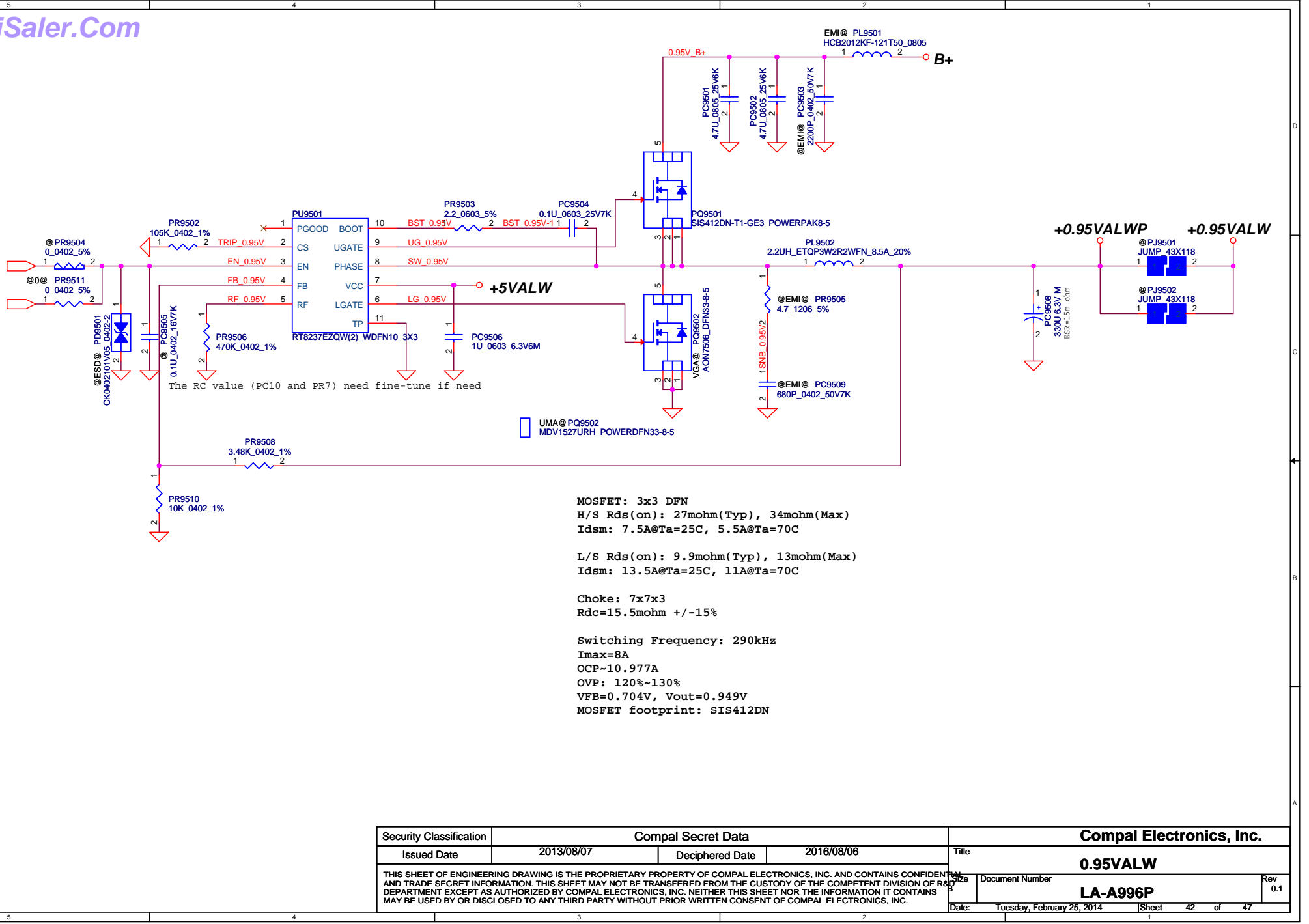




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Issued Date	2013/08/07	Deciphered Date	2016/08/06	1.35V/0.675VSP	
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				LA-A521P	
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Issued Date	2013/08/07	Deciphered Date	2016/08/06	Title
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Document Number				Rev
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Date:			Sheet	41 of 47



Saler.Com

The RC value (PC10 and PR7) need fine-tune if need

UMA@PQ9502
MDV1527URH_POWERDFN33-8-5

MOSFET: 3x3 DFN
H/S Rds(on): 27mohm(Typ), 34mohm(Max)
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds(on): 9.9mohm(Typ), 13mohm(Max)
Idsm: 13.5A@Ta=25C, 11A@Ta=70C

Choke: 7x7x3
Rdc=15.5mohm +/-15%

Switching Frequency: 290kHz
Imax=8A
OCP~10.977A
OVP: 120%~130%
VFB=0.704V, Vout=0.949V
MOSFET footprint: SIS412DN

Security Classification		Compal Secret Data		Title	
Issued Date	2013/08/07	Deciphered Date	2016/08/06	0.95VALW	
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0.95VALW

+5VALW

+0.95VALWP

+0.95VALW

UMA@ PQ9502
MDV1527URH_POWERDFN33-8-5

MOSFET: 3x3 DFN
H/S Rds(on): 27mohm(Typ), 34mohm(Max)
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds(on): 9.9mohm(Typ), 13mohm(Max)
Idsm: 13.5A@Ta=25C, 11A@Ta=70C

Choke: 7x7x3
Rdc=15.5mohm +/-15%

Switching Frequency: 290kHz
Imax=8A
OCP~10.977A
OVP: 120%~130%
VFB=0.704V, Vout=0.949V
MOSFET footprint: SIS412DN

Security Classification
Compal Secret Data

Issued Date
2013/08/07

Deciphered Date
2016/08/06

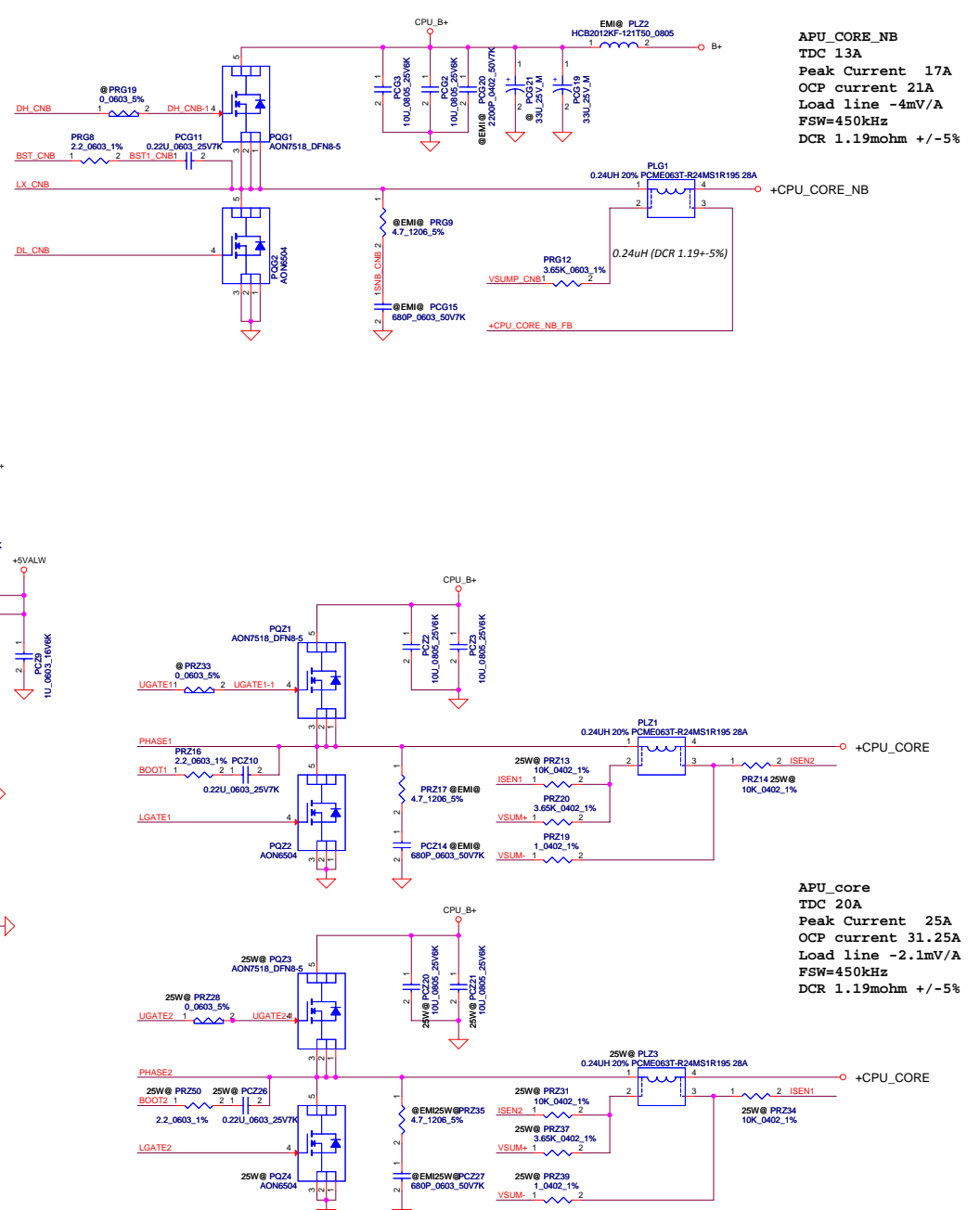
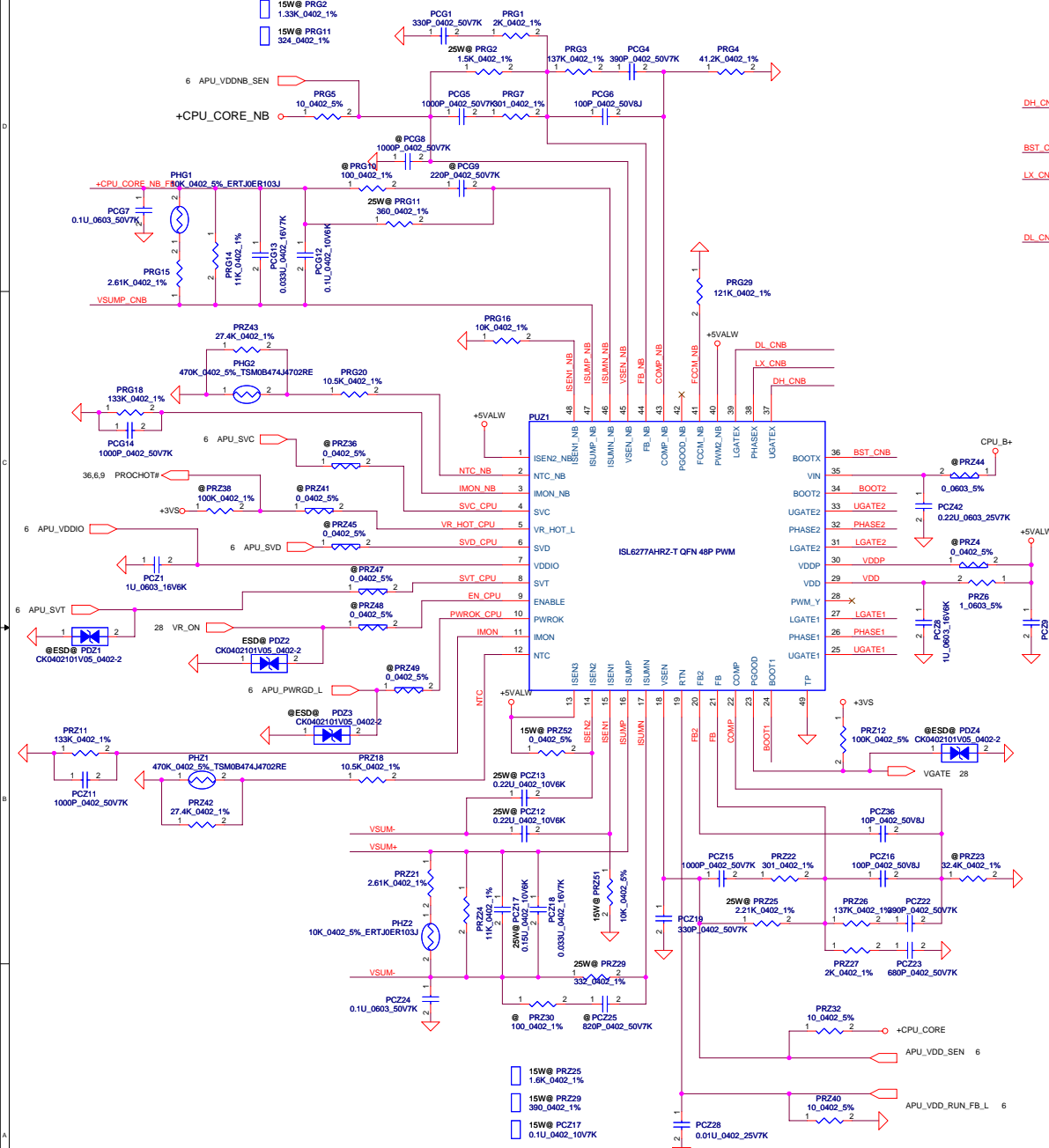
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Document Number
LA-A996P

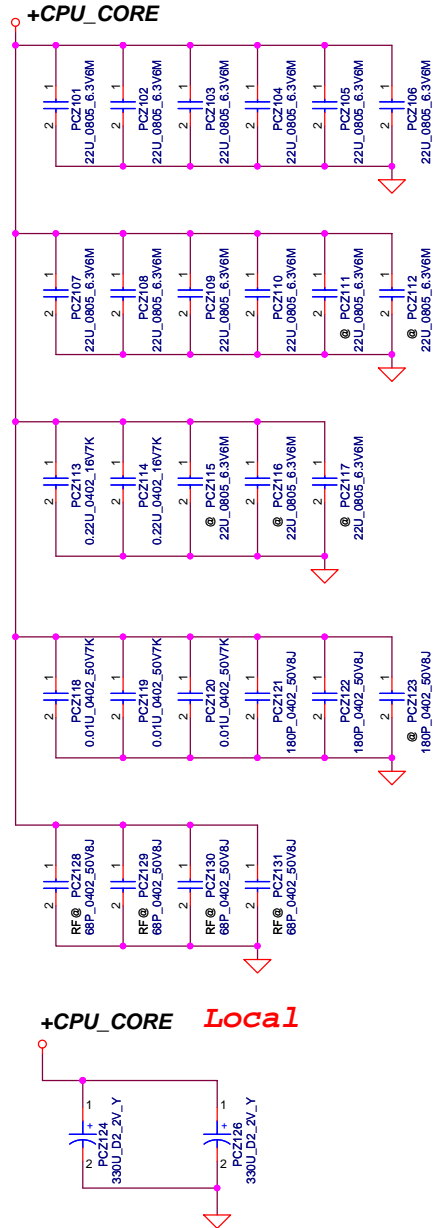
Rev
0.1

Date: Tuesday, February 25, 2014 **Sheet** 42 **of** 47

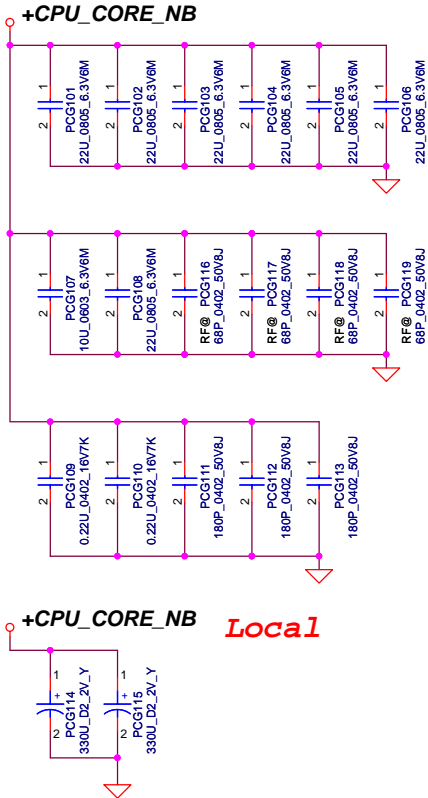
- 15W@ PRG2
1.33K_0402_1%
- 15W@ PRG11
324_0402_1%



+CPU_CORE



+CPU_CORE_NB



	330uF/9m	22uF/0805	0.22uF/0402	10uF/0603	0.01uF/0402	180pF/0402
+CPU_CORE	2	10	2		3	2
+CPU_CORE_NB	2	7	2	1		3

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GPI021	GPI029	GPI030	GPI020	GPI015	
VID5	VID4	VID3	VID2	VID1	VDDC
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

Vboot(merge)

Layout Note:
PWL should place near Choke

H-side MOS:SIR472DP
Rds(on):
12mohm @ Vgs=10V
15mohm @ Vgs=4.5V
Id :20A @Ta=25 degC

L-side MOS:MDU1511RH
Rds(on):
2.0mohm(typ) & 2.4mohm(max) @ Vgs=10V
2.7mohm(typ) & 3.3mohm(max) @ Vgs=4.5V
Id :100A @Ta=25 degC

Choke: 0.36uH (Size:10*10*4)
Rdc=1.1mohm +5%
Heat Rating Current=33A
Saturation Current=39A

Output Cap: 10mohm * 560uF * 3 pcs

Remark:

- Rbias=147K
=>set the controller for CPU_CORE application
Rbias=47k
=>set the controller for GPU_CORE application
- Switching frequency setting:
 $f_{set}(kohm)=\frac{1}{period(us)} \cdot 0.29 \cdot 2^6.5$
=8.06kohm
 $F_{sw}=1/period(us)=300KHZ$
- Operation mode:
when GPU_CORE VR application
DPRSLPVR (pin28)=0 => 1 phase CCM mode
DPRSLPVR (pin28)=1 => 1 phase DE mode

TDC: 21A
Peak Current = 31.5A
OCP Current = 37.8A
Load line disable

Module model information:
ISL62881C_V1A for IC
ISL62881C_V1B for SW

Security Classification		Compal Secret Data		Title	
Issued Date	2013/08/07	Deciphered Date	2016/08/06	Document Number	LA-A996P
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Date:	Tuesday, February 25, 2014	Sheet	45	of	47

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GPI021	GPI029	GPI030	GPI020	GPI015	
VID5	VID4	VID3	VID2	VID1	VDDC
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

Vboot(merge)

Remark:

- Rbias=147K
=>set the controller for CPU_CORE application
Rbias=47k
=>set the controller for GPU_CORE application
- Switching frequency setting:
 $f_{\text{set}}(\text{kohm}) = \frac{1}{\text{period}(\mu\text{s}) - 0.29} * 2.65$
=8.06kohm
 $f_{\text{sw}} = 1/\text{period}(\mu\text{s}) = 300\text{KHZ}$
- Operation mode:
when GPU_CORE VR application
DPRSLPVR (pin28)=0 => 1 phase CCM mode
DPRSLPVR (pin28)=1 => 1 phase DE mode

Vboot regulation

Module model information:
ISL62881C_V1A for IC
ISL62881C_V1B for SW

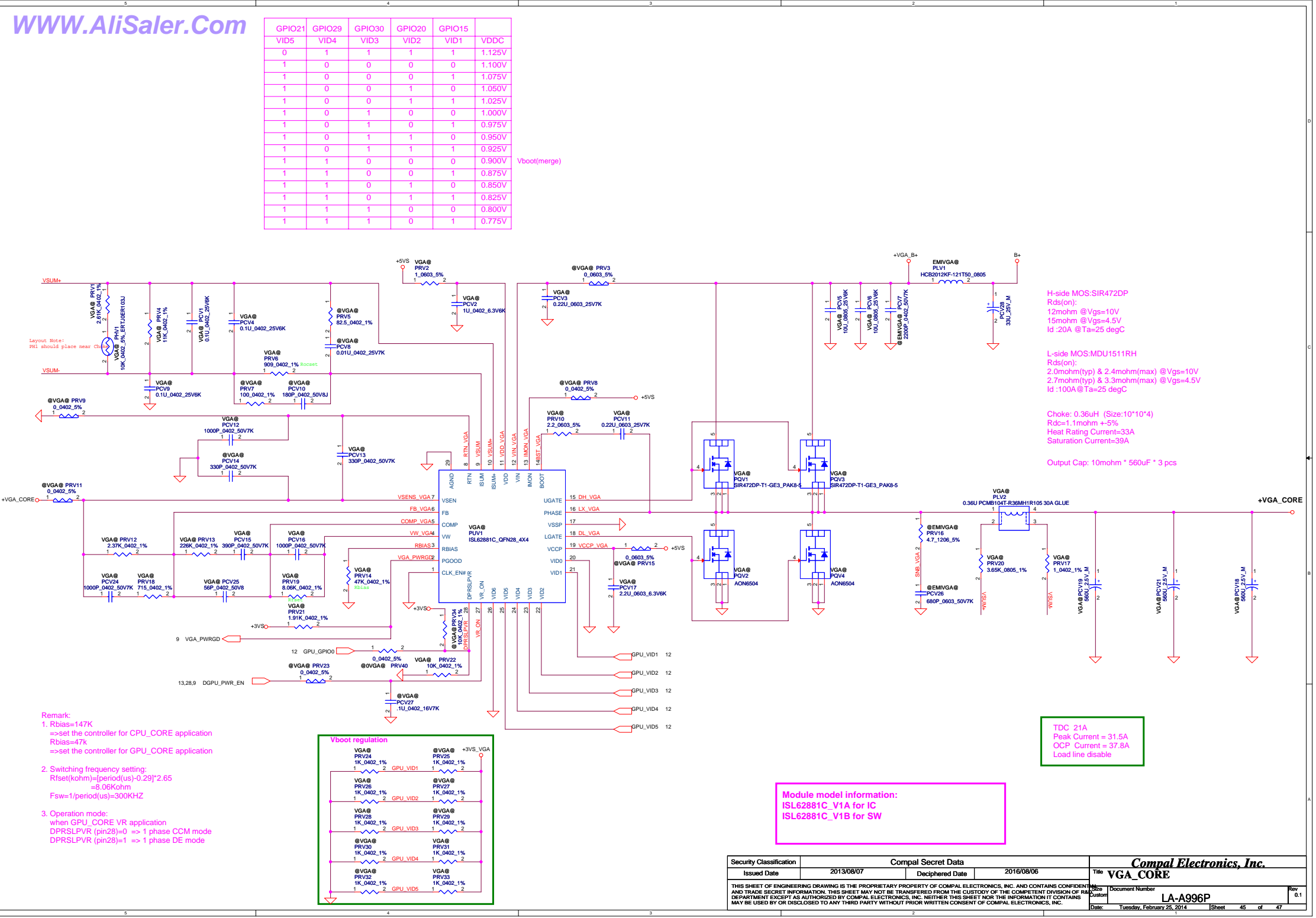
TDC 21A
Peak Current = 31.5A
OCP Current = 37.8A
Load line disable

Security Classification

Issued Date	Deciphered Date	Document Number	Title
2013/08/07	2016/08/06	LA-A996P	VGA_CORE

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GPIOD1	GPIOD9	GPIOD30	GPIOD20	GPIOD15	
VID5	VID4	VID3	VID2	VID1	VDDC
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

Vboot(merge)

Remark:

- Rbias=147K
=>set the controller for CPU_CORE application
Rbias=47k
=>set the controller for GPU_CORE application
- Switching frequency setting:
 $f_{set}(kohm) = \frac{1}{period(us)} - 0.29 * 2^6$
=8.06Kohm
 $Fsw = \frac{1}{period(us)} = 300KHZ$
- Operation mode:
when GPU_CORE VR application
DPRSLPVR (pin28)=0 => 1 phase CCM mode
DPRSLPVR (pin28)=1 => 1 phase DE mode

Vboot regulation

Module model information:
ISL62881C_V1A for IC
ISL62881C_V1B for SW

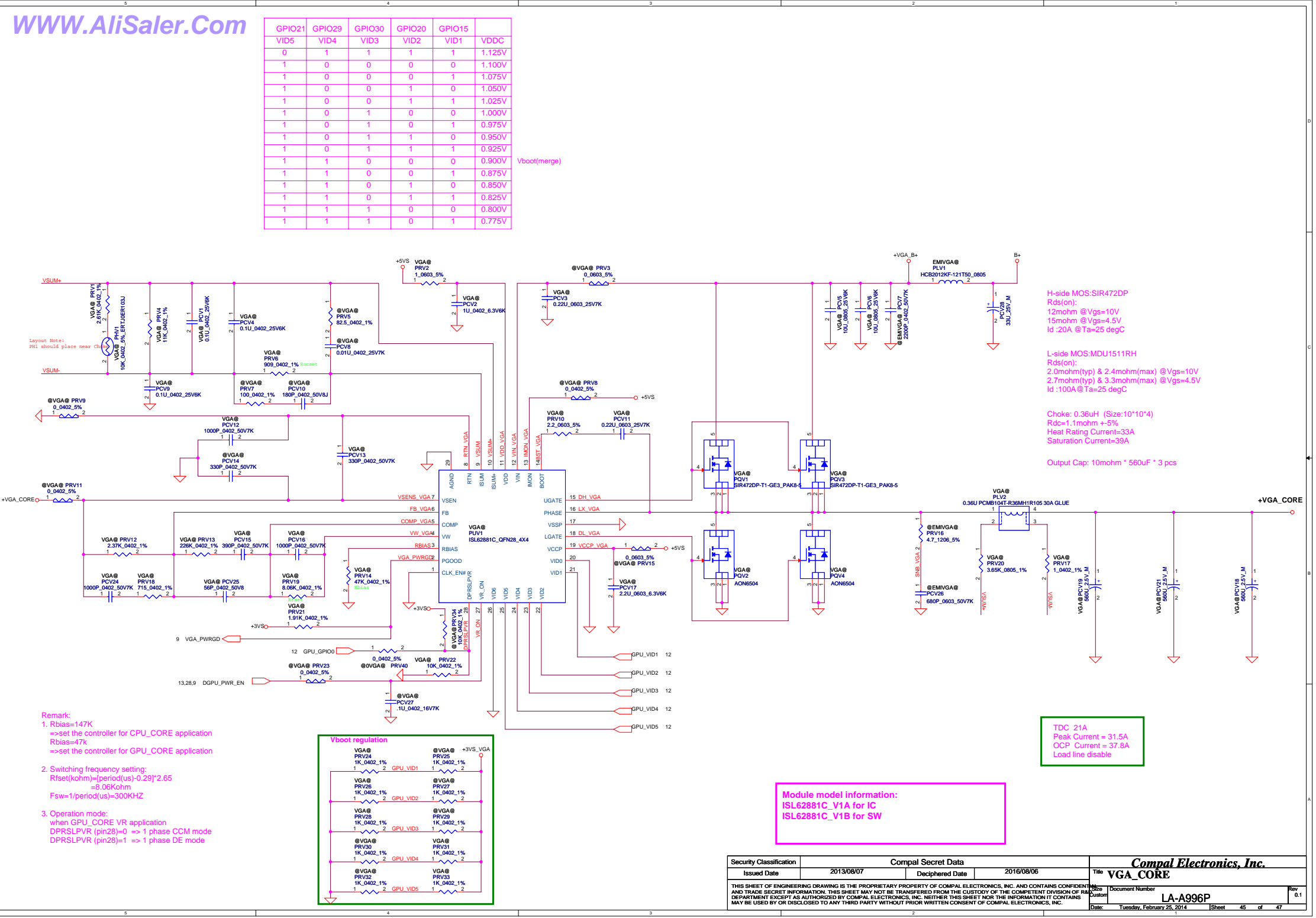
TDC 21A
Peak Current = 31.5A
OCP Current = 37.8A
Load line disable

Security Classification

Issued Date	Deciphered Date	Document Number	Title
2013/08/07	2016/08/06	LA-A996P	VGA_CORE

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Date: Tuesday, February 25, 2014 Sheet 45 of 47



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GPI021	GPI029	GPI030	GPI020	GPI015	
VID5	VID4	VID3	VID2	VID1	VDDC
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

Vboot(merge)

Remark:
 1. Rbias=147K
 =>set the controller for CPU_CORE application
 Rbias=47k
 =>set the controller for GPU_CORE application
 2. Switching frequency setting:
 $Rfset(kohm) = \frac{period(us)}{0.29} * 2.65$
 $= 8.06 Kohm$
 $Fsw = 1 / period(us) = 300 KHZ$
 3. Operation mode:
 when GPU_CORE VR application
 DPRSLPVR (pin28)=0 => 1 phase CCM mode
 DPRSLPVR (pin28)=1 => 1 phase DE mode

Vboot regulation

VGA@ PRV24	@VGA@ PRV25	+3VS_VGA
1K_0402_1%	1K_0402_1%	1 2
1 2	1 2	
VGA@ PRV26	@VGA@ PRV27	
1K_0402_1%	1K_0402_1%	1 2
1 2	1 2	
VGA@ PRV28	@VGA@ PRV29	
1K_0402_1%	1K_0402_1%	1 2
1 2	1 2	
VGA@ PRV30	@VGA@ PRV31	
1K_0402_1%	1K_0402_1%	1 2
1 2	1 2	
VGA@ PRV32	@VGA@ PRV33	
1K_0402_1%	1K_0402_1%	1 2
1 2	1 2	

Module model information:
 ISL62881C_V1A for IC
 ISL62881C_V1B for SW

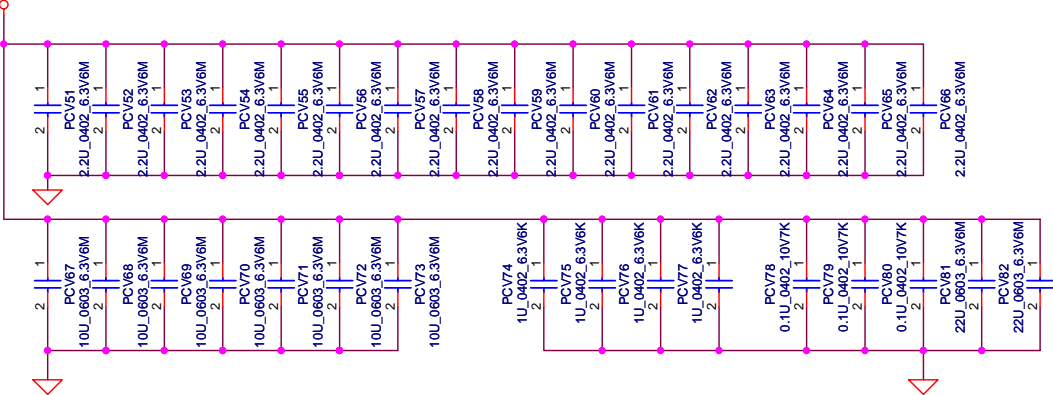
TDC 21A
 Peak Current = 31.5A
 OCP Current = 37.8A
 Load line disable

Security Classification
 Issued Date: 2013/08/07
 Deciphered Date: 2016/08/06
 Title: **VGA_CORE**
 Document Number: LA-A996P
 Revision: 0.1
 Date: Tuesday, February 25, 2014
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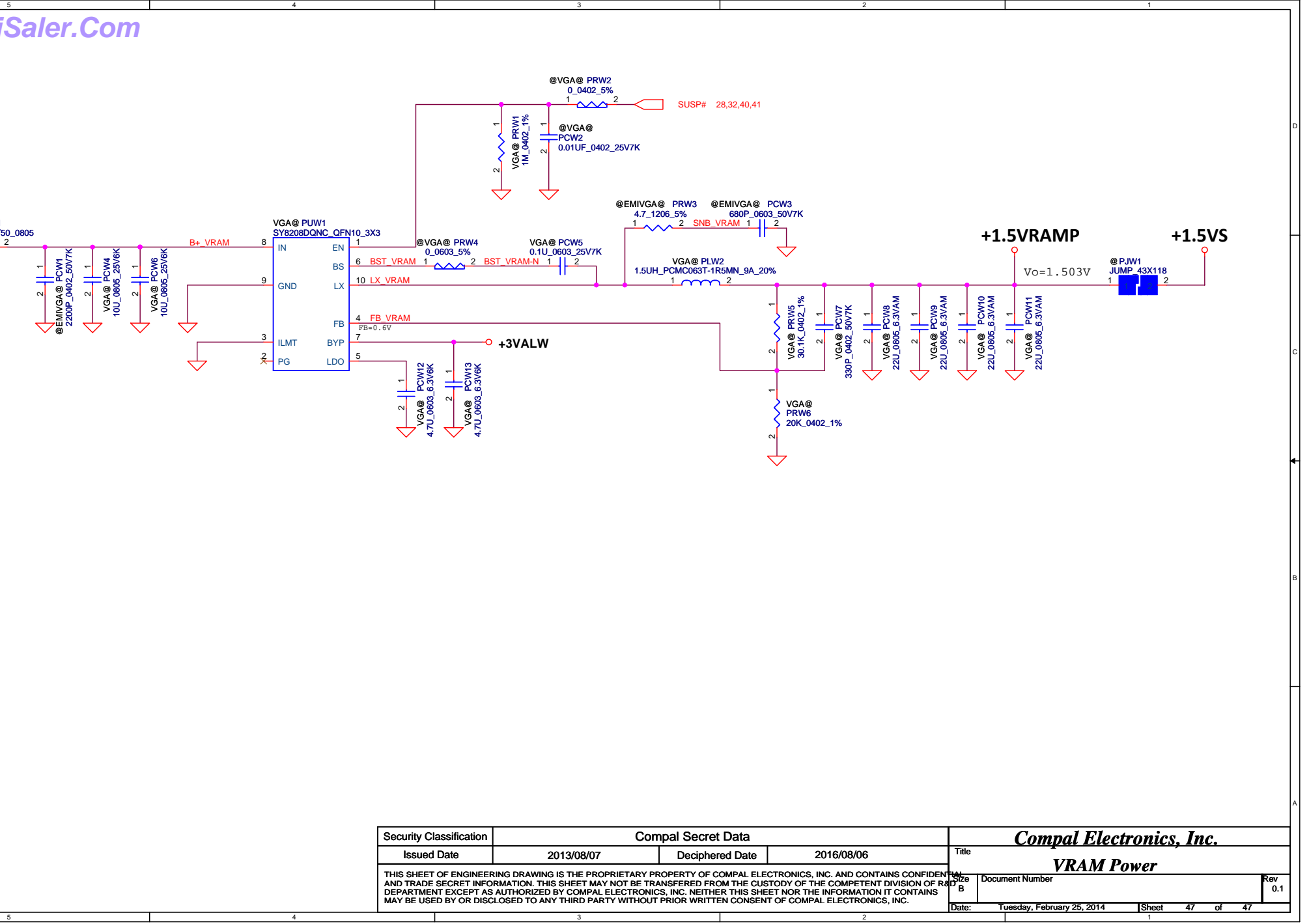
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The schematic diagram illustrates the VGA CORE circuit, featuring a central IC (ISL62881C) and various peripheral components. The circuit includes a Vboot regulation section, a main power supply section, and a signal processing section. Key components include resistors (e.g., 10K, 1K, 100K, 100P), capacitors (e.g., 0.1uF, 0.01uF, 0.001uF, 0.0001uF), and integrated circuits (e.g., ISL62881C, PCV1, PCV2, PCV3, PCV4, PCV5, PCV6, PCV7, PCV8, PCV9, PCV10, PCV11, PCV12, PCV13, PCV14, PCV15, PCV16, PCV17, PCV18, PCV19, PCV20, PCV21, PCV22, PCV23, PCV24, PCV25, PCV26, PCV27, PCV28, PCV29, PCV30, PCV31, PCV32, PCV33, PCV34, PCV35, PCV36, PCV37, PCV38, PCV39, PCV40, PCV41, PCV42, PCV43, PCV44, PCV45, PCV46, PCV47, PCV48, PCV49, PCV50, PCV51, PCV52, PCV53, PCV54, PCV55, PCV56, PCV57, PCV58, PCV59, PCV60, PCV61, PCV62, PCV63, PCV64, PCV65, PCV66, PCV67, PCV68, PCV69, PCV70, PCV71, PCV72, PCV73, PCV74, PCV75, PCV76, PCV77, PCV78, PCV79, PCV80, PCV81, PCV82, PCV83, PCV84, PCV85, PCV86, PCV87, PCV88, PCV89, PCV90, PCV91, PCV92, PCV93, PCV94, PCV95, PCV96, PCV97, PCV98, PCV99, PCV100, PCV101, PCV102, PCV103, PCV104, PCV105, PCV106, PCV107, PCV108, PCV109, PCV110, PCV111, PCV112, PCV113, PCV114, PCV115, PCV116, PCV117, PCV118, PCV119, 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PCV495, PCV496, PCV497, PCV498, PCV499, PCV500, PCV501, PCV502, PCV503, PCV504, PCV505, PCV506, PCV507, PCV508, PCV509, PCV510, PCV511, PCV512, PCV513, PCV514, PCV515, PCV516, PCV517, PCV518, PCV519, PCV520, PCV521, PCV522, PCV523, PCV524, PCV525, PCV526, PCV527, PCV528, PCV529, PCV530, PCV531, PCV532, PCV533, PCV534, PCV535, PCV536, PCV537, PCV538, PCV539, PCV540, PCV541, PCV542, PCV543, PCV544, PCV545, PCV546, PCV547, PCV548, PCV549, PCV550, PCV551, PCV552, PCV553, PCV554, PCV555, PCV556, PCV557, PCV558, PCV559, PCV560, PCV561, PCV562, PCV563, PCV564, PCV565, PCV566, PCV567, PCV568, PCV569, PCV570, PCV571, PCV572, PCV573, PCV574, PCV575, PCV576, PCV577, PCV578, PCV579, PCV580, PCV581, PCV582, PCV583, PCV584, PCV585, PCV586, PCV587, PCV588, PCV589, PCV590, PCV591, PCV592, PCV593, PCV594, PCV595, PCV596, PCV597, PCV598, PCV599, PCV600, PCV601, PCV602, PCV603, PCV604, PCV605, PCV606, PCV607, PCV608, PCV609, PCV610, PCV611, PCV612, PCV613, PCV614, PCV615, PCV616, PCV617, PCV618, PCV619, PCV620, PCV621, PCV622, PCV623, PCV624, PCV625, PCV626, PCV627, PCV628, PCV629, PCV630, PCV631, PCV632, PCV633, PCV634, PCV635, PCV636, PCV637, PCV638, PCV639, PCV640, PCV641, PCV642, PCV643, PCV644, PCV645, PCV646, PCV647, PCV648, PCV649, PCV650, PCV651, PCV652, PCV653, PCV654, PCV655, PCV656, PCV657, PCV658, PCV659, PCV660, PCV661

+VGA_CORE



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Issued Date	2013/08/07	Deciphered Date	2016/08/06	Title	VGA CHIP DECOUPLING
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				Rev	0.1
Date:				Tuesday, February 25, 2014	Sheet 46 of 47



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The schematic diagram illustrates the VRAM Power circuit for the SY8208DQNC QFN10_3X3 component. The circuit is powered by a +3VALW input and a +1.5VRAMP output. The output voltage is Vo=1.503V. The circuit includes various capacitors (PCW1-PCW11, PRW1-PRW6, PLW2) and resistors (PCW1-PCW11, PRW1-PRW6, PLW2). The output voltage is Vo=1.503V.

Security Classification		Compal Secret Data		Title	
Issued Date	2013/08/07	Deciphered Date	2016/08/06	VRAM Power	
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Date:	Tuesday, February 25, 2014	Sheet	47 of 47	Rev	0.1